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CONCEPTION D'UN RÉSEAU DE PLOTS CONFIGURABLES MULTI-FONCTIONS ANALOGIQUES ET NUMÉRIQUES COMBINÉ À UN RÉSEAU DE DISTRIBUTION DE PUISSANCE INTÉGRÉS À L'ÉCHELLE DE LA TRANCHE DE SILICIUM

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ÉCOLE POLYTECHNIQUE DE MONTRÉAL

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Cette thèse intitulée :

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présentée par : LAFLAMME-MAYER Nicolas

en vue de l'obtention du diplôme de : Philosophiae Doctor

a été dûment acceptée par le jury d'examen constitué de :

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RÉSUMÉ

De nos jours, les systèmes électroniques sont en constante croissance en taille et en complexité. Cette complexité combinée à la réduction du temps de mise en marché rendant le design de systèmes électroniques un grand défi pour les designers. Une plateforme de prototypage a récemment été introduite afin de s'attaquer toutes ces contraintes à la fois. Cette plateforme s'appuie sur l'implémentation d'un circuit configurable à l'échelle d'une tranche de silicium complète de 200mm de diamètre. Cette surface est recouverte d'une mer de plots conducteurs configurables appelés NanoPads.

Ces NanoPads sont suffisamment petits pour supporter des billes d'un diamètre de 250 µm et d'un espacement de 500 µm et sont regroupés en matrices de 4×4 pour former des Cellules, qui sont à leur tour assemblées en Réticules de 32×32. Ces Réticules sont ensuite photo-répétés sur toute la surface d'une tranche de silicium et sont interconnectés entre eux pour former le WaferIC. Cet arrangement particulier de plots conducteurs configurables permet à un usager de déposer sur la surface active du WaferIC les circuits intégrés constituant un système électronique, sans tenir en compte l'orientation spatiale de ces derniers, de créer un schéma d'interconnexions, de distribution la puissance et de débuter le prototypage du système en question. Une version préliminaire a été fabriquées et testées avec succès et permet d'alimenter des circuits -intégrés et de configurer le WaferIC pour les interconnecter.

Cette thèse par articles présente une nouvelle version du WaferIC avec une nouvelle proposition de distribution de la puissance avec une approche de maîtres-esclaves qui met en valeur l'utilisation de plusieurs rails d'alimentation afin d'améliorer le rendement énergétique. Il est également mis de l'avant un réseau très dense de convertisseurs analogique-numérique (CAN) et numérique-analogique (CNA) de plus de 300k éléments, tolérant aux défectuosités et aux défauts de fabrication. Ce réseau de CAN-CNA permet d'améliorer le WaferIC avec la transmission de signaux analogiques, en plus des signaux numériques.

Ce manuscrit comporte trois articles : un publié chez « *Springer Science & Business Media Analog Integrated Circuits and Signal Processing* », un publié chez « *IEEE Transactions on Circuits and Systems I : Regular Papers* » et finalement un soumis chez « *IEEE Transactions on Very Large Scale Integration* ». Dans ces articles de nouvelles architectures de régulateurs linéaires à double rails d'alimentation, de tampons analogiques configurables et de références de

tensions configurables applicable à un CNA y sont présentées et décrites. Une nouvelle approche de distribution de la puissance en plus de l'intégration de toutes les nouvelles architectures y est également présentée sous forme d'une puce d'essai en technologie CMOS 0.18 µm intégrant une version miniature du WaferIC.

L'ajout d'un second rail d'alimentation pour les régulateurs linéaires permet de diminuer les pertes thermiques dans le silicium. L'architecture proposées se démarque du fait qu'elle partage plusieurs sous-circuits ce qui la rend compact et possible à intégrer dans l'espace sur-contraint du WaferIC, tout en offrant des bonnes performances lorsque comparée à la littérature.

Le tampon analogique configurable, la référence de tension et les convertisseurs se démarquent car ceux-ci partagent tous les mêmes circuits. La réutilisation du tampon analogique et de la référence de tension configurable, un convertisseur numérique-analogique et par le fait même un convertisseur analogique-numérique.

La contribution majeure est l'intégration et la réutilisation de circuits menant à une cellule de NanoPads comprenant deux régulateurs linéaires à double rails d'alimentations, de deux CAN et deux CNA intégrant un système de redondance tolérants aux défectuosités, de deux références de tension configurable ainsi que 16 E/S numériques configurables, le tout dans une surface de silicium ultra-compact.

ABSTRACT

Nowadays, electronic systems are in constant growth, size and complexity; combined with time to market it makes a challenge for electronic system designers. A prototyping platform has been recently introduced and addresses all those constraints at once. This platform is based on an active 200 mm in diameter wafer-scale circuit, which is covered with a set of small configurable and conductive pads called NanoPads.

These NanoPads are designed to be small enough to support any integrated-circuit µball of a 250 µm diameter and 500 µm of pitch. They are assembled in a 4×4 matrix, forming a Unit-Cell, which are grouped in a Reticle-Image of 32×32. These Reticle-Images are photo-repeated over the entire surface of a 200 mm in diameter wafer and are interconnected together using inter-reticle stitching. This active wafer-scale circuit is called a WaferIC. This particular topology and distribution of NanoPads allows an electronic system designer to manually deposit any integrated-circuit (IC) on the active alignment insensitive surface of the WaferIC, to build the netlist linking all the ICs, power-up the systems and start the prototyping of the system.

In this manuscript-based thesis, we present an improved version of the WaferIC with a novel approach for the power distribution network with a master-slave topology, which makes the use of embedded dual-power-rail voltage regulators in order to improve the power efficiency and decrease thermal dissipation. We also propose a default-tolerant network of analog to digital (ADC) and digital to analog (DAC) converters of more than 300k. This ADC-DAC network allows the WaferIC to not only support digital ICs but also propagate analog signals from one NanoPad to another. This thesis includes 3 papers : one submission to "*Springer Science & Business Media Analog Integrated Circuits and Signal Processing*", one submission to "IEEE Transactions on Circuits and Systems I : Regular Papers" and finally one submission to "IEEE Transactions on Very Large-Scale Integration". These papers propose novel architectures of dual-rail voltage regulators, configurable analog buffers and configurable voltage references, which can be used as a DAC. A novel approach for a power distribution network and the integration of all the presented architectures is also proposed with the fabrication of a testchip in CMOS 0.18 µm technology, which is a small-scale version of the WaferIC.

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CAO	Conception Assistée par Ordinateur
CI	Circuit intégré
TSV	Through Silicon Via
NP	NanoPad
CU	Cellule-Unitaire
SR	Switching Regulator
LDO	Low Dropout Regulator
PSR	Power Supply Rejection
PTAT	Proportional To Absolute Temperature
CTAT	Complementary To Absolute Temperature
CNA	Convertisseur Numérique à Analogique
CAN	Convertisseur Analogique à Numérique

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CHAPITRE 1 INTRODUCTION

1.1 Description du projet

La conception de systèmes numériques complexes nécessite un flot de conception pouvant requérir plusieurs mois voire des années/personnes de travail. Le design doit être élaboré, implémenté, déverminé, amélioré pour finalement entrer en production. Plusieurs outils permettant d'accélérer leur développement existent tel que les FPGA, les émulateurs matériels, les outils de conception assistés par ordinateur, les microcontrôleurs. Cependant, ces derniers n'accélèrent ou n'améliorent pas tous les aspects, négligeant la conception et la fabrication du support pour le système numérique désiré, soit le circuit imprimé. Aucun outil à ce jour n'a pu intégrer tous ces aspects.

Une plateforme de prototypage de systèmes numériques complexes a récemment fait son apparition. Bénéficiant d'une intégration à l'échelle de la tranche de silicium « *wafer-scale* », cette dernière permet d'assister le designer, de la conception jusqu'au déverminage du système. Pouvant être comparé à un circuit imprimé reconfigurable, cet outil de conception permet d'interconnecter tous les circuits intégrés constituant le système à développer, de lui fournir la puissance nécessaire via un réseau de distribution de puissance également configurable, échanger des signaux autant numériques qu'analogiques et de pouvoir communiquer avec le monde externe.

Le circuit intégré à l'échelle de la tranche, WaferIC^{TM}, est constitué d'une mer de plots configurables disposés de manière régulière. Plus de 1.2 M de plots, appelé NanoPad, recouvrent la surface du WaferIC et sont regroupés en matrice 4×4 formant une cellule mesurant 560 µm × 560 µm. Les cellules regroupées en matrices de 32×32 couvrent ainsi un réticule qui est photo-répété76 fois sur toute la surface d'une tranche de silicium de 200 mm de diamètre, formant ainsi le WaferIC. La Figure 1.1 explique l'architecture hiérarchique du WaferIC. Cette architecture permet à un usager de déposer un arrangement de circuits intégrés (CI) constituant le système numérique à concevoir, de définir les interconnexions entre ces derniers, d'y appliquer la puissance nécessaire et de débuter la phase de test et de prototypage sans devoir concevoir de support physique tel un circuit imprimé.

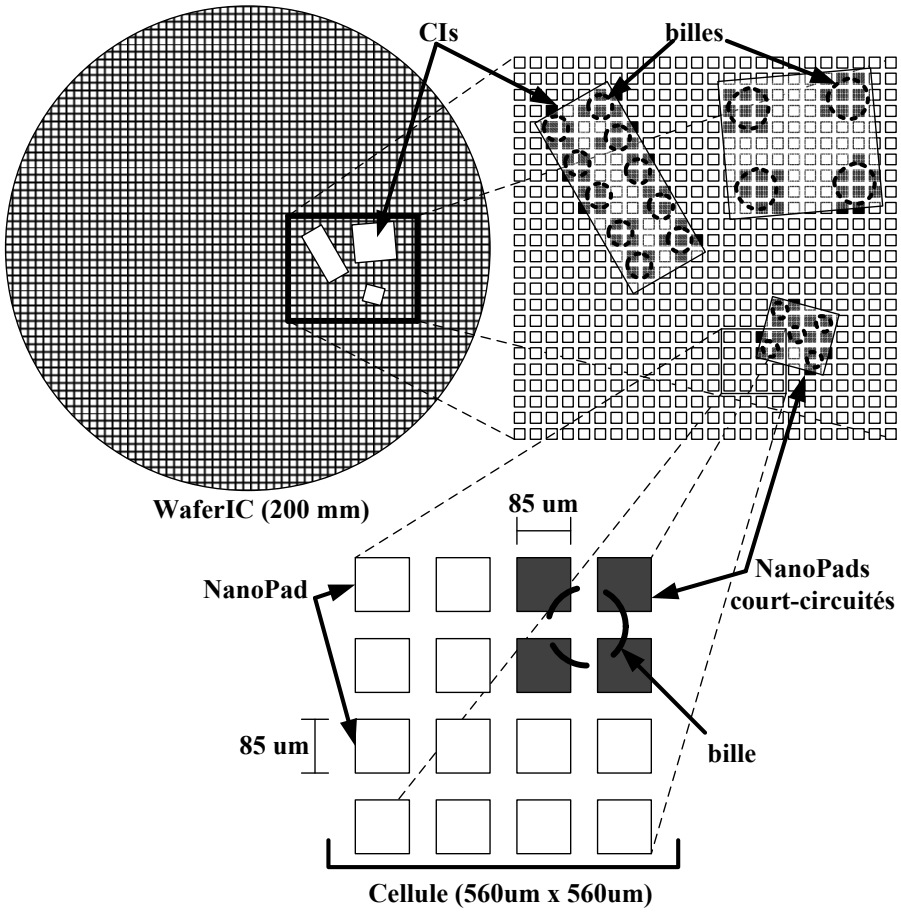


Figure 1.1 Description du WaferIC à partir d'un réticule jusqu'au Nanopad où plusieurs circuits intégrés sont déposés et court-circuitent plusieurs NanoPads

Afin de supporter un maximum de circuits intégrés, les plots recouvrant le WaferIC doivent être en mesure de s'adapter à la tâche requise : une entrée/sortie numérique ou analogique, une tension régulée configurable, haute -impédance ou une mise à la terre. La conception d'un tel plot comporte bien des défis puisque chaque type de configuration possède ses caractéristiques qui lui sont propres : vitesse, bande passante, puissance de sortie, plage dynamique, impédance de sortie ou d'entrée et bien plus. Une version préliminaire a été publiée dans la revue « *Transactions on Very Large-Scale Integreation »,* et a été fabriquée et testée. Cette version se veut une approche minimaliste pouvant fournir de la puissance n'utilisant qu'une seule tension d'alimentation, soit 3.3 V, et ne pouvant agir en tant qu'entrée/sortie numérique. La circuiterie de cette version du plot configurable occupe la totalité de la surface de silicium disponible.

1.2 Objectifs de recherche

L'objectif principal de recherche de la présente thèse de doctorat est de proposer une architecture nouvelle au niveau Cellule et NanoPad permettant l'ajout de nouvelles fonctionnalités, puisque la version préliminaire se limite qu'aux circuits intégrés numériques. De plus, la distribution de puissance ne s'effectuant que d'un rail d'alimentation de 3.3 V entraîne des points chauds où les contraintes thermiques atteignent leurs limites pour des tensions régulées basses tel que 1.0 V, puisque l'efficacité d'un régulateur linéaire est directement proportionnelle à sa tension d'alimentation (efficacité $\approx V_{OUT}/V_{IN}$).

Les objectifs spécifiques de cette thèse se résument aux points suivants :

1 Investiguer et proposer un régulateur linéaire à double rails d'alimentation de 1.8 et 3.3V n'utilisant aucun réservoir capacitif externe, dans la même surface de silicium que la version préliminaire.

2 Investiguer et proposer un générateur de tension configurable sur une large plage de valeurs possédant un ajustement fin de la tension de sortie, dans une surface de silicium compacte et pouvant être réutilisé comme convertisseur numérique-analogique (CNA).

3 Investiguer et proposer un réseau de distribution de puissance hiérarchique permettant de libérer un maximum de surface de silicium permettant l'intégration de toutes les nouvelles fonctionnalités dans le but de concevoir une puce d'essai se voulant une version miniature du WaferIC.

1.3 Contributions à la recherche

Dans cette thèse de doctorat, quatre articles sont présentés :

1 N. Laflamme-Mayer, Y. Blaquière, Y. Savaria and M. Sawan, " A Configurable Multi-Rail Power and I/O Pad Applied to Wafer-Scale Systems," *IEEE Transactions on Circuits and Systems-I Regular paper- publié en novembre 2014.*

2 N. Laflamme-Mayer, Y. Blaquière and M. Sawan, " A Configurable Analog Buffer Dedicated to a Wafer-Scale Prototyping Platform,"*Springer Science & Business Media Analog Integrated Circuits and Signal Processing- publié en Janvier 2015.*

3 N. Laflamme-Mayer, Y. Blaquière, Y. Savaria and M. Sawan, " A Fault-Tolerant Network of a sea of SAR-ADCs and DAC based on an Unbalanced Buffer Technique," *IEEE Transactions on Very Large Scale Intergration – soumis le 13 septembre 2017.*

4 N. Laflamme-Mayer, Y. Blaquière, Y. Savaria and M. Sawan, " A Fully Configurable and Integrated Pad Dedicated to an Active Interposer Technology," *IEEE Transactions on Very Large Scale Integration- soumis prochainement.*

Le premier article propose un régulateur linéaire à tension de sortie configurable comportant plusieurs rails d'alimentation et intégrant une entrée/sortie (E/S) numérique. Une boucle de rétroaction commune pouvant être adaptée à la tension d'alimentation souhaitée y est proposée. Un puce d'essai incorporant deux rails de 1.8 et 3.3 V a été fabriquée en technologie CMOS 0.18 µm et occupe une surface de 0.008 mm^2 pour des tensions de sorties régulées pouvant varier de 500 mV jusqu'à 2.955 V avec un courant maximal de 40 mA. Ce plot incorpore également une E/S numérique à tension de sortie configurable de 500 mV à 2.955 V qui peut atteindre une vitesse de transmission de 250 MHz (ou également 250 Mbits/s). La contribution majeure de cet article est le partage de circuiteries entres les différents rails d'alimentation ainsi que sa surface de silicium compact en conversant toutefois des performances comparables à la littérature.

Le deuxième article est une invitation suite à une publication à la conférence « Latin American Symposium on Circuits and Systems (LASCAS 2013) de l'article « *A configurable analog buffer dedicated to a wafer-scale prototyping platform of electronic systems* ». Cet article porte sur un tampon de sortie analogique pouvant être configuré quant à son courant de consommation statique (ou courant de polarisation) ainsi que son temps de montée et de descente. Ceci permet de diminuer l'injection de bruit dans l'alimentation et permet également une meilleure gestion du courant de consommation global du WaferIC lors de son intégration au niveau de la tranche de silicium. Ce tampon analogique permet d'atteindre une bande passante allant jusqu'à 194 MHz pour une surface de silicium totale de 0.001824 mm^2. La contribution majeure de cet article est la

proposition d'un design compact simple et pouvant être réutiliser dans plusieurs applications dans l'optique du WaferIC.

Le troisième article propose une approche innovatrice afin de produire une tension de sortie configurable sur une large plage de valeurs avec un ajustement fin de cette tension. Une puce d'essai en technologie CMOS 0.18 µm a été fabriquée et se veut une version miniature du WaferIC. Basée sur une paire différentielle débalancée, cette approche permet d'étendre une tension fixe de 2.5 V, générée par un circuit de type « *bandgap* », de 0.85 V jusqu'à 2.538 V avec une résolution de 8-bits pour un ajustement fin de 25 mV. Cette approche est étendue pour constituer un CNA de 10 MS/s avec un nombre effectif de bit de 7.6, possédant une rejection du bruit par rapport au signal (SNR) de 51.87 dB ainsi qu'une plage dynamique de 42.31 dB, le tout dans une surface de 0.00035 mm^2. Ce CNA est la pièce maîtresse de la propagation de signaux analogiques dans le WaferIC, où un réseau de CAN (de type approximations-successives) et de CNA tolérant aux pannes y sont proposés.

Le quatrième article présente le réseau de distribution de la puissance y incorporant un réseau de type maîtres-esclaves de régulateurs linéaires à double rails d'alimentation où plusieurs NanoPads partagent un seul et même régulateur. Cette approche permet une meilleure utilisation de la surface de silicium disponible, permettant l'intégration du bus analogique présenté dans le 3^{e} article ainsi que des E/S numériques présentés dans le 1er article. Cette architecture, destinée au WaferIC, fait également une extension à la technologie des « *interposers* » 2.5D et 3D où un circuit actif à l'échelle de la tranche de silicium configurable et adaptatif y est proposé. Cette technologie est l'empilage de plusieurs circuits intégrés entre lesquels on y dépose un « interposer » qui a comme fonctions d'interconnecter ceux-ci entre eux, de manière passive (ex. connexions métalliques) ou de manière active (ex. distribution de puissance).

1.4 Disposition de la thèse

Ce manuscrit comporte huit chapitres où chacun des quatre articles y sont présentés dans les chapitres 3, 4, 5 et 6. Suivant la présente introduction, la thèse est structurée comme suit :

- Le chapitre 2 décrit en détails le WaferIC quant à son architecture et ses contraintes. Une revue de la littérature s'en suit concernant les différentes architectures et designs de régulateurs linéaires à un seul ou plusieurs rails d'alimentation. S'en suit une revue des

différentes architectures de CNA et de CAN ainsi que de générateurs de tension configurable. Une brève exploration de divers bus analogiques y est également effectuée.

- Les chapitres 3 à 6 font l'objet des 4 articles de journaux, mentionnés précédemment, présentés dans leur intégralité et précédés d'un court résumé de la contribution de chacun ainsi que des résultats qui y sont présentés.
- Le chapitre 7 présente une discussion générale de la thèse de doctorat et fait une synthèse de l'accomplissement des divers objectifs décrits lors de l'introduction.
- Le chapitre 8 conclu ce manuscrit et y suggère différentes pistes de travaux futurs pouvant enrichir d'avantage ces travaux de recherche.

CHAPITRE 2 REVUE DE LA LITTÉRATURE

Dans ce chapitre nous aborderons le WaferIC, qui se veut un circuit et une approche unique. De cette description découleront les besoins du WaferIC qui feront ensuite objet d'une revue de littérature plus approfondi pour chacun des types de circuits nécessaires. Il y a tout d'abord la distribution de la puissance à l'aide de régulateurs linéaires, les références de tensions configurables ou non ainsi que les convertisseurs analogique/numérique et numérique/analogique.

Ce chapitre débute par la présentation et la description du WaferIC au niveau structurel, les contraintes qui y sont associées ainsi que la problématique avec la version préliminaire du WaferIC. S'en suit une revue des architectures et des différents types de designs de régulateurs linéaires qui pullulent dans la littérature. Quelques architectures où plusieurs tensions d'alimentation sont utilisées sont également abordées. Une description des différents travaux explorés quant aux références de tension configurables ainsi que des travaux publiés concernant les diverses approches de bus analogiques y sont finalement présentés. Une revue des quatre grandes familles de convertisseurs analogique-numérique suit : « *flash, pipeline, successive-approximation, oversampling* ». Une approche semblable décrit ensuite les grands types de convertisseurs numérique-analogique : « *resistive ladder, curren tsteering, current steering binary weighted, charge scaling* ». Un retour est ensuite effectué afin de bien positionner les travaux de cette thèse qui ont menés à l'exploration de nouveaux circuits et architectures.

2.1 Le WaferIC

2.1.1 Fonctionnement globale du WaferIC

Le WaferIC se veut un circuit totalement reconfigurable où tous les plots à sa surface peuvent se comporter de manière à pouvoir s'interconnecter avec n'importe quel circuit intégré qui y serait déposé (E/S, puissance, etc.). En y déposant, sur la surface active du WaferIC, les circuits intégrés constituant un système numérique complexe (FPGA, mémoire, processeur, etc.) un usager peut, grâce à un vaste réseau d'interconnexions numériques, créer les liens numériques entre les divers circuits intégrés, y appliquer la puissance nécessaire et débuter le prototypage et

le déverminage du design. La Figure 2.1 montre un exemple minimaliste ou 3 circuits -intégrés sont déposés à la surface du WaferIC et interconnectés.

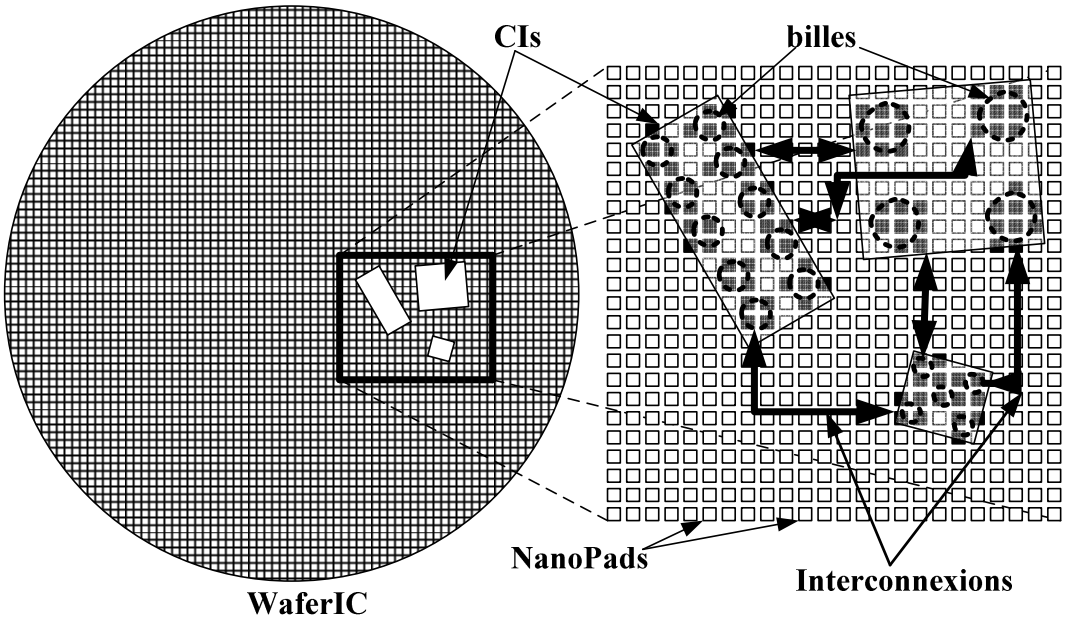


Figure 2.1 Exemple de système numérique où plusieurs circuits intégrés déposés à la surface du WaferIC sont interconnectés pour former un système numérique à prototyper.

2.1.2 Le NanoPad et le CPAD

Le WaferIC est un circuit actif configurable à l'échelle de la tranche de silicium. Il est recouvert d'une mer de plots configurables appelés NanoPads, qui constituent le plus petit élément du WaferIC. Chacun des NanoPads est un point de connexion physique (plot métallique) pouvant entrer en contact avec une bille d'un circuit-intégré. Ce plot métallique mesurant 85 µm×85 µm se situe au-dessus d'une surface de silicium comportant des circuits actifs permettant la configuration du NanoPad selon le type de bille qui serait en contact avec ce dernier comme le montre la Figure 2.2 (Norman, Valorge, Blaquière, Lepercq, Basile-Bellavance, & El-Alaoui, 2008). Ces circuits-actifs configurables sont appelés CPADs, où un CPAD est de taille 110 µm×77 µm et peut s'interconnecter physiquement au NanoPad disposé au-dessus de lui. En d'autres termes, le NanoPad se retrouve à être le point d'interconnexion physique avec le monde externe (bille) et le CPAD, les circuits actifs permettant la configuration du NanoPad selon le type de bille en contact avec ce dernier : tension régulée, E/S numérique ou analogique, mise à la

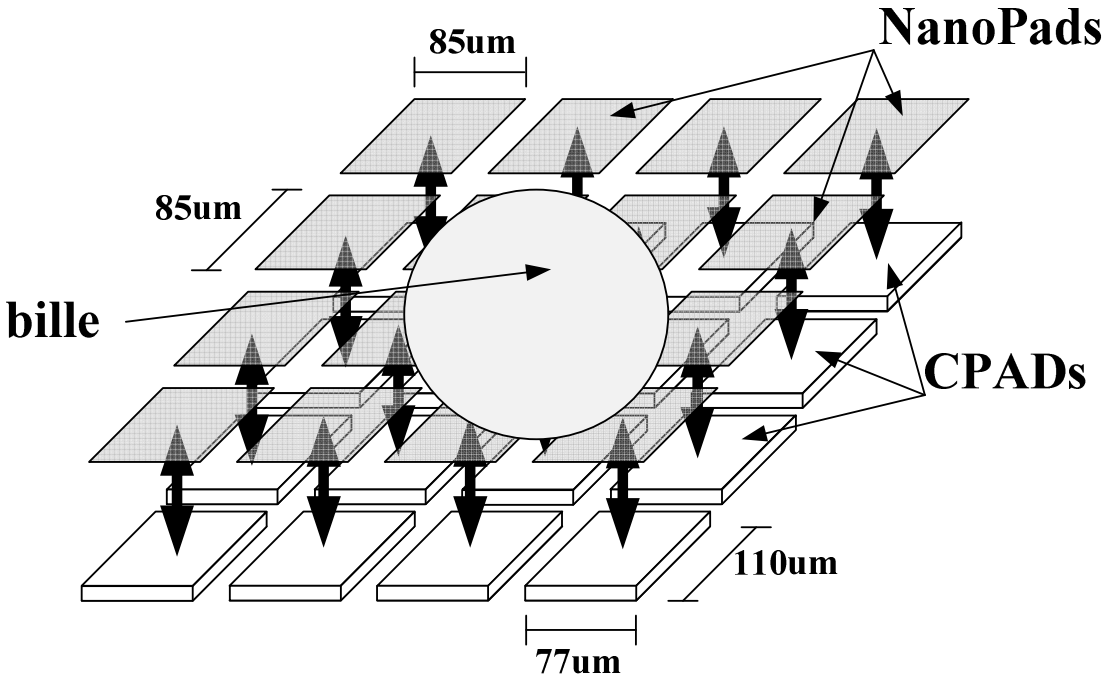


Figure 2.2 Description du lien entre les NanoPads et les CPADs constituant le WaferIC ainsi que leurs tailles respectives (Laflamme-Mayer, André, Valorge, Blaquière, & Sawan, 2013).

terre, haute-impédance. La différence de taille entre les CPADs et les NanoPads provient du fait que la surface de silicium active est partagée entre les CPADs et d'autres circuits permettant sa configuration et son bon fonctionnement. La non-régularité de la taille des CPADs est uniformisée à l'aide de la dernière couche de métal disponible de la technologie visée.

2.1.3 Architecture hiérarchique du WaferIC

Le WaferIC est recouvert de 1 245 185 NanoPads uniformément distribués sur l'intégralité de la surface d'une tranche de silicium de 200 mm de diamètre. Un regroupement de 16 NanoPads disposés en matrices de 4×4 forment une Cellule qui est à son tour sont regroupé en matrices 32×32 ce qui constitue l'élément de base du WaferIC. Cet élément, appelé Réticule, est ensuite photo-répété 76 fois sur toute la surface de la tranche de silicium et les réticules sont interconnectés ensemble via un procédé de « *inter-reticle stitching* ». La Figure 2.3 montre la vue hiérarchique du WaferIC jusqu'au NanoPads.

La surface du WaferIC est exempte de toute structure mécanique ou autre et est recouverte d'un film conducteur à axe vertical, un « *Z-axis film* » (Diop, Radji, Hamoui, Blaquière, & Izquierdo, 2013). Ce film a pour fonction de protéger mécaniquement la surface fragile du WaferIC lorsqu'une ou plusieurs billes y sont déposées, ainsi que d'assurer un bon contact électrique entre la dite bille et les NanoPads, comme le montre la Figure 2.4.

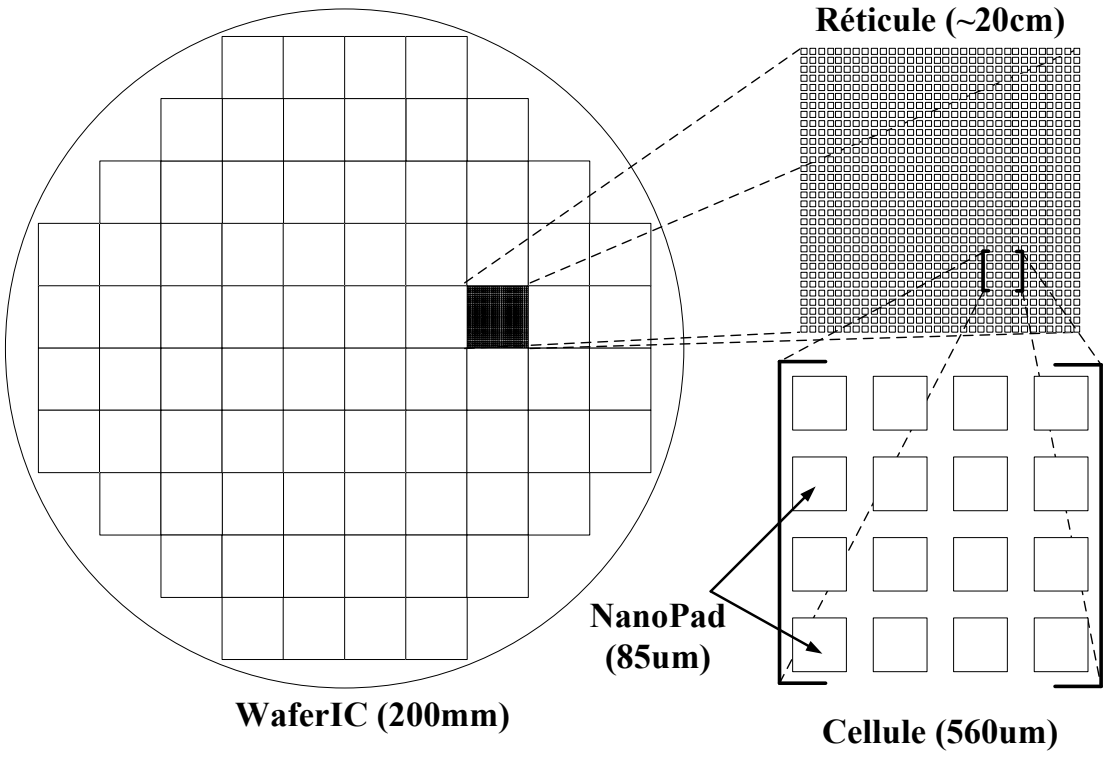


Figure 2.3 Vue hiérarchique du WaferIC jusqu'au NanoPads

2.1.4 Réseau de distribution de la puissance du WaferIC

Le réseau de puissance du WaferIC est un réseau en arborescence où la puissance totale fournie par la racine est un circuit-imprimé effectuant une première conversion AC/DC pour générer des tensions de 0 V et +12 V. Ces deux tensions sont ensuite propagées à l'ensemble du WaferIC à l'aide de 19 modules discrets, appelés Power-Bloc. Ces modules sont l'interface physique entre le wafer lui-même et le monde externe, fournissant la puissance ainsi que les signaux nécessaires à la configuration et le fonctionnement du WaferIC. Les puissances fournies à la tranche de silicium sont 0 V, 1.8 V et 3.3 V pour un total de 5 A et 20 A pour les tensions de 1.8 V et 3.3 V respectivement. Chaque Power-Bloc peut alimenter jusqu'à 4 réticules simultanément. Le

transfert de puissance d'un Power-Bloc au WaferIC s'effectue au moyen de « *Through Silicon Via* » (TSV). Puis, une grille intégrée propage les trois tensions (0V, 1.8 V et 3.3 V) à tout le Réticule (Valorge, Andrée, Savaria, & Blaquière, 2011). Seul la mise à la terre (0 V) est commune à tous les Réticules du WaferIC afin d'assurer une référence commune entre les différents réticules, les alimentations 1.8 et 3.3 V sont quant à elles indépendantes d'un Réticule à l'autre. Les NanoPads sont les feuilles de ce réseau en arborescence, où à leur tour, ils fourniront de la puissance régulée à une bille (Laflamme-Mayer, André, Valorge, Blaquière, & Sawan, 2013). La Figure 2.5et Figure 2.6 montrent la structure du réseau de distribution de puissance de la racine (circuit-imprimé) jusqu'au WaferIC.

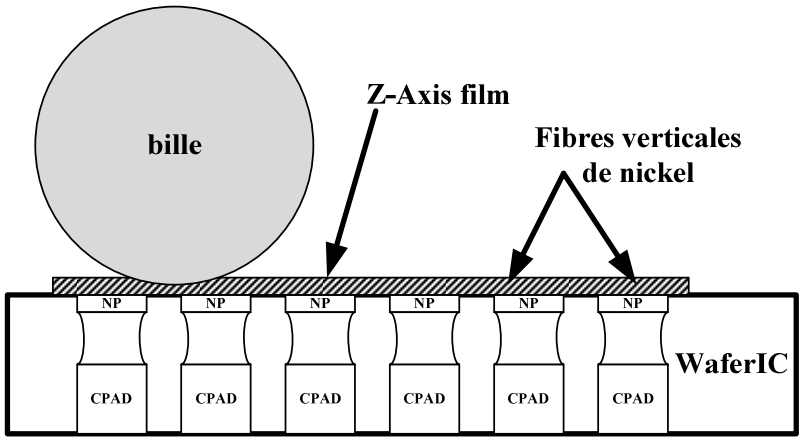


Figure 2.4 Figure explicative montrant le « *Z-axis film* » protégeant la surface du WaferIC et permettant un bon contact électrique grâce à sa structure en fibres verticales conductrices de nickel.

2.1.5 Propagation de signaux dans le WaferIC

Le WaferIC peut propager des signaux numériques d'un NanoPad à n'importe quel autre en utilisant un réseau dense d'interconnexions appelé WaferNet. Se basant sur une Cellule, qui comporte 16 NanoPads, celle-ci peut simultanément propager 2 signaux en entrée et deux signaux en sortie vers le WaferNet. Ces signaux peuvent se propager de Cellule en Cellule dans les quatre directions, soit nord, sud, est et ouest par des liens de longueur 1, 2, 4, 8, 16 ou 32 cellules, comme le montre la Figure 2.7. Un lien de longueur 1 signifie que le dit signal numérique à propager est communiqué à la Cellule immédiatement voisine, un lien de longueur

2, à son deuxième voisin et ainsi de suite pour les autres liens (Lepercq, Valorge, Basile-Bellavance, Laflamme-Mayer, Blaquière, & Savaria, 2009).

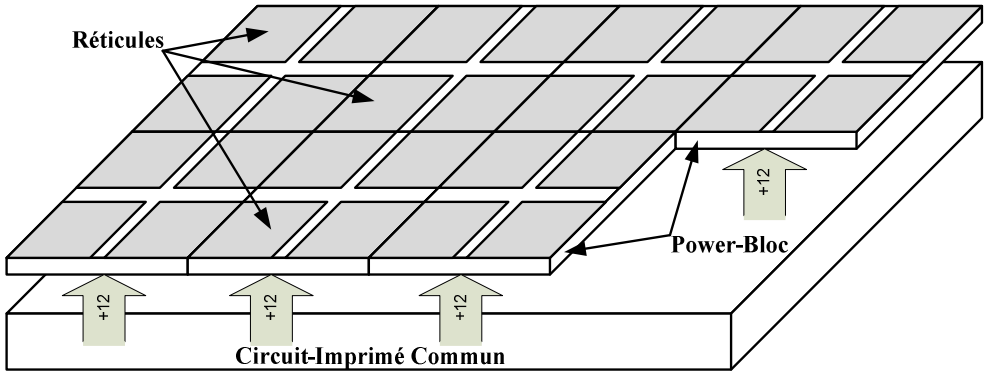


Figure 2.5 Distribution de la puissance en arborescence d'un circuit-imprimé commun aux Réticules via des Power-Bloc.

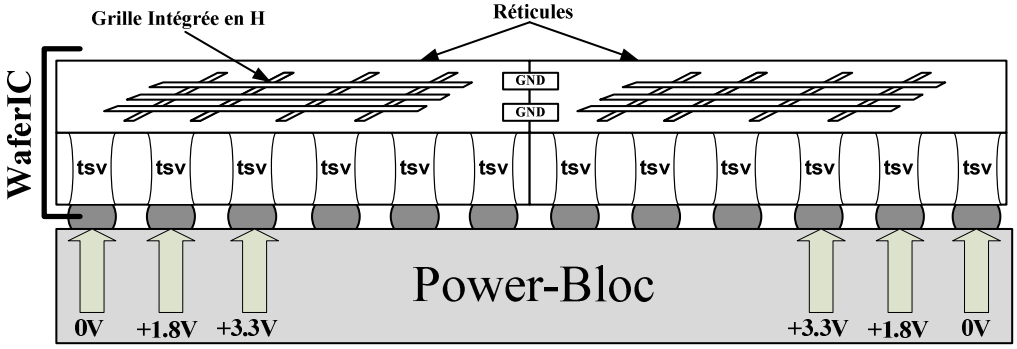


Figure 2.6 Distribution de la puissance d'un Power-Bloc vers une grille de métal intégrée distribuant la puissance dans un Réticule.

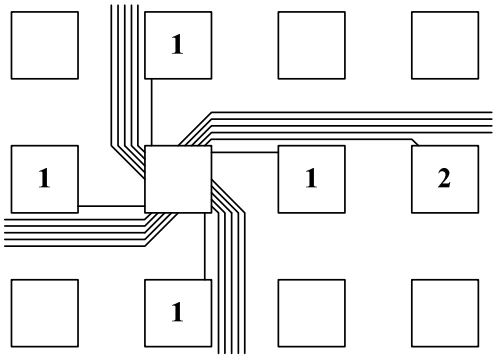


Figure 2.7 WaferNet pouvant propager des signaux numériques dans toutes les directions (N-S-E-O) avec des liens de longueur couvrant 1, 2, 4, 8, 16 et 32 cellules.

2.1.6 Contraintes associées au WaferIC

La topologie particulière du WaferIC impose des contraintes physiques associées aux choix architecturaux. L'intégration de type « *wafer-scale* » implique également des contraintes supplémentaires quant à la surface de silicium ainsi qu'à la consommation.

2.1.6.1 Contraintes physiques du WaferIC

Les contraintes physiques découlent des choix architecturaux du WaferIC quant à la taille d'une Cellule et d'un NanoPad. Ces derniers ont été sélectionnés afin de supporter des billes d'un diamètre de 250 µm et d'un espacement allant jusqu'à 500 µm (Norman, Valorge, Blaquière, Lepercq, Basile-Bellavance, & El-Alaoui, 2008).Ces tailles de billes sont les tailles associées aux plus petits boitiers de type « *BGA* ». Une seconde contrainte architecturale est de pouvoir supporter jusqu'à 2 billes différentes par Cellule (Norman, Valorge, Blaquière, Lepercq, Basile-Bellavance, & El-Alaoui, 2008). Cette dernière contrainte provient d'une étude réalisée afin de déterminer le nombre de liens maximal possible au WaferNet dans une surface de silicium donnée. Ces deux contraintes fixent la taille d'une Cellule à 560 µm×560 µm.

La taille des NanoPads a été choisie en fonction d'obtenir un taux de remplissage maximal de la surface du WaferIC. Cependant, plus le nombre de NanoPads est important, plus la surface de silicium nécessaire pour les implémenter et les configurer le sera également. L'étude effectuée en (Norman, Valorge, Blaquière, Lepercq, Basile-Bellavance, & El-Alaoui, 2008) a démontrée qu'une matrice 4×4 était optimale, ce qui fixe la taille d'un NanoPad à 85 µm×85 µm. La surface de silicium associée à chaque CPAD est légèrement supérieure à celle d'un NanoPad soit de 110 µm×77 µm, représentant 43.2 % de la surface de silicium disponible pour une Cellule. Le restant de l'espace est attribué aux autres circuits nécessaires pour sa configuration et son fonctionnement ainsi que le WaferNet.

Tableau 2.1 Résumé des différentes contraintes physiques associées au WaferIC

Nombre de NanoPads	1 245 184
Taille d'un NanoPad	85 µm×85 µm (0.007225 mm^2)
Taille d'un CPAD	110 µm×77 µm (0.00847 mm^2)
Taille d'une Cellule	560 µm×560 µm (0.3136 mm^2)
Taille d'un Réticule	17.92 mm×560 mm (321.1264 mm^2)

2.1.6.2 Contraintes de puissance et de tension de sortie du WaferIC

Les contraintes décrites dans la section précédente définissent l'espace disponible, en parlant de surface de silicium, pour y implémenter les fonctionnalités nécessaires afin qu'un NanoPad puisse être configuré pour accommoder tous les types de bille avec laquelle il pourrait entrer en contact. Une bille peut soit nécessiter une puissance régulée sous forme d'une tension, soit être une entrée/sortie analogique ou numérique. Le réseau de distribution de puissance du WaferIC fournit au Cellules, et du même coup aux CPADs, deux tensions de 1.8 et 3.3 V tel que décrit dans la section 2.1.4. Les niveaux de tensions régulées ainsi que les possibles niveaux de tension de sortie numérique et analogique doivent donc se retrouver à l'intérieur de ces deux niveaux. Le courant fourni par la version préliminaire du WaferIC en (Laflamme-Mayer, André, Valorge, Blaquière, & Sawan, 2013) est de 110 mA par CPAD pour une tension régulée et est de 4 mA pour un plot numérique en sortie.

L'intégration à très grande échelle du WaferIC apporte des contraintes supplémentaires quant à la consommation statique des circuits. Une consommation de courant statique de 100 µA pour un CPAD entraîne un courant statique pour le WaferIC de plus de 120 A. En contrepartie, une diminution trop importante de ce courant statique entraînerait des pertes de performance importantes. Chaque CPAD doit donc pouvoir être mis hors tension au besoin.

2.1.7 Résumé des contraintes et particularités du WaferIC

En résumé des sections précédentes, le WaferIC est constitué de 1 245 184 NanoPads d'une taille de 85µm×85µm et d'une surface active de 110 µm×77 µm. Les NanoPads sont regroupés en

matrices de 4×4 et forment une Cellule de 560 µm×560 µm. Ces Cellules sont alimentées du bas vers le haut, utilisant la technologie des *TSV*, avec des tensions de 0 V, 1.8 V et 3.3 V. Chaque Cellule possède 2 liens numériques en entrée et deux liens en sortie qui sont partagés par les 16 CPADs la constituant. Chaque CPAD doit pouvoir être configuré, pour se connecter avec tous types de bille d'un circuit-intégré : fournir une tension régulée, être un plot d'entrée/sortie numérique ou analogique.

2.2 Description de la problématique

2.2.1 Effet thermique de la distribution de la puissance

La version actuelle du WaferIC n'utilise qu'un seul rail d'alimentation (3.3 V) pour fournir la puissance aux circuits intégrés déposés à la surface de ce dernier. Puisque seuls des régulateurs linéaires sont possibles à intégrer dans la surface de silicium disponible, l'efficacité de la distribution de puissance est directement reliée à la tension régulée. De plus, puisque les CI sont très fréquemment alimentés à plus basse tension (cœur des circuits) et que les E/S sont alimentées à plus haute tension, la majeure partie de la puissance requise est donc à faible tension où le rendement est le plus faible. Prenons l'exemple d'un FPGA avec un cœur alimenté à 1.2 V et des E/S à 2.5 V. Le rendement théorique maximal pour un système à un seul rail à 3.3 V n'est que de 36 %. En contrepartie un rail d'alimentation à 1.8 V augmente ce rendement à 67 %. Cette amélioration du rendement se traduit directement par une puissance moindre à évacuer sous forme de chaleur. Pour un circuit consommant 10 W à 1.2 V ayant les mêmes rendements, un rail à 1.8 V signifie une économie de puissance de plus de 12 W.

Pour améliorer le rendement de la distribution de la puissance, un second rail d'alimentation devrait être utilisé. Cependant, l'ajout de ce rail revient à doubler l'espace occupé par les régulateurs intégrés, ce qui n'est pas possible. Une nouvelle architecture doit être avancée afin de pouvoir bénéficier des deux rails disponibles (1.8 V et 3.3 V) tout en conservant dans le pire des cas la même surface de silicium occupée.

2.2.2 Niveaux de tensions disponibles

La version actuelle du WaferIC ne dispose que d'un nombre discret de niveaux de tensions, soit les niveaux CMOS standards de 1.0, 1.2, 1.5, 1.8, 2.0, 2.5 et 3.3 V. Cette approche se veut

conservatrice quant à la surface de silicium employée entraînant en contrepartie certaines limitations. Aucun ajustement fin ne peut être effectué, tel que l'augmentation ou diminution de ladite tension pour pallier à une chute de tension trop sévère due à un mauvais partage de la puissance (CI déposés trop près l'un de l'autre) ou bien dus aux changements de température ou aux variations de procédés au travers toute la tranche de silicium de 200 mm. D'autant plus que des tensions fixes limitent le WaferIC quant au support éventuel de nouveaux CIs ayant des tensions d'alimentation différentes ainsi que des circuits purement analogiques.

2.2.3 Propagation de signaux analogiques

La conception d'un système numérique complexe nécessite, en plus de liens numériques rapides, la possibilité de propager des signaux purement analogiques. La version actuelle du WaferIC ne le permet tout simplement pas. Plusieurs approches peuvent être abordées, mais presque toutes se résument à une conversion dans le domaine numérique et à une reconstruction du signal désiré. Dans tous les cas, une surface de silicium importante (relativement à l'espace disponible du WaferIC) est requise. Une architecture qui réutilise les transistors et circuits disponibles serait une approche intéressante.

Dans la même suite d'idées, la propagation de signaux analogiques, l'intégration de convertisseurs analogique/numérique (CAN) et de convertisseurs numérique/analogique (CNA) sont des ajouts importants dans la conception et le déverminage de systèmes numériques complexes. Le WaferIC doit donc être en mesure d'échantillonner le niveau de tension de tous les NanoPads présents. Un système unique revient à intégrer plus de 1.2 M de CAN et de CNA, ce qui est très improbable étant donné la surface disponible. Une architecture de partage avec un nombre plus limité de convertisseurs est donc requise. De plus, ces convertisseurs pourraient également être réutilisés dans l'optique de propager des signaux analogiques.

2.3 Revue des régulateurs linéaires

Il existe deux types de régulateurs, les régulateurs linéaires de type « *Low-Dropout Regulator (LDO)* » et de type *« switching regulator* » (SR). Bien que les régulateurs SR puissent offrir un rendement très intéressant de l'ordre de 95 %, il n'en demeure pas moins qu'ils nécessitent des composantes externes difficiles voire impossibles à intégrer (Hazucha, Karnik, Bloechel, Parsons,

Finan, & Borkar, 2005). Puisqu'une solution compacte, où la surface de silicium est l'enjeu majeur de cette thèse, la présente proposition ne se concentrera que sur les régulateurs linéaires.

2.3.1 Régulateurs linéaires de type source-commune

Un régulateur linéaire typique est montré à la Figure 2.8où un amplificateur d'erreur commun est utilisé afin de comparer la tension régulée avec une référence vref. Cette technique permet d'obtenir de faibles variations de la tension de sortie mais offre une rejection du bruit de l'alimentation plutôt médiocre en plus d'avoir une largeur de bande fréquentielle limitée due à l'utilisation d'un amplificateur opérationnel (Hazucha, Karnik, Bloechel, Parsons, Finan, & Borkar, 2005). De plus, ce type d'approche nécessite très fréquemment une capacité de découplage qui peut atteindre plusieurs µF.

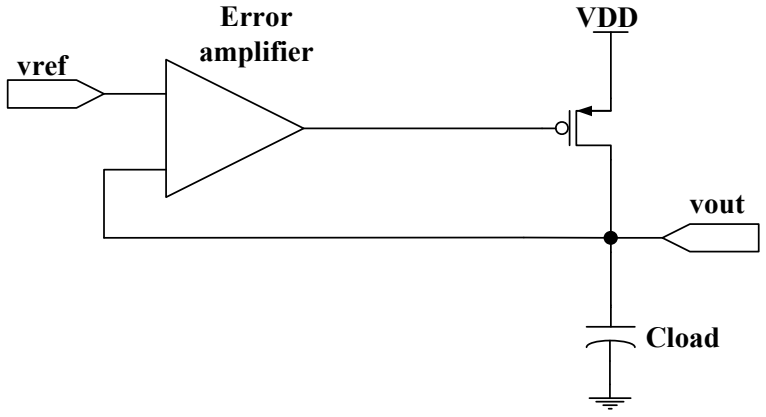


Figure 2.8 Régulateur linéaire conventionnel.

2.3.2 Compensation fréquentielle avec placement de pôles et de zéros

Une amélioration du LDO typique (Figure 2.8) consiste à créer un zéro à l'intérieur de la boucle de rétroaction plutôt que de se fier à celui généré par la charge équivalente résistive sériel (ESR) et à la capacité de charge (Cload). Cette technique permet de contrôler précisément les caractéristiques du zéro ajouté afin de minimiser les écarts de tension de types « *overshoot* » et « *undershoot* » lorsque le LDO est en fonction. Ajouter un duo de pôle-zéros où le zéro est à plus basse fréquence comme le montre la Figure 2.9a pour effet d'améliorer la marge de phase. Toutefois, cette approche nécessite l'intégration d'une capacité de l'ordre de 5 nF (Chava & Silva-Martinez, 2004).

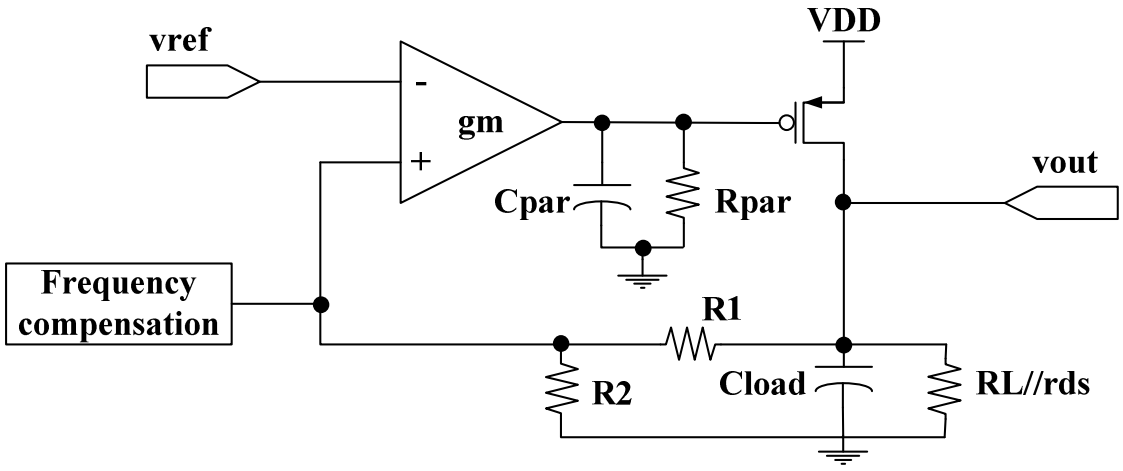


Figure 2.9 LDO à compensation fréquentielle par ajout d'un duo pôle-zéros dans la boucle de rétroaction (Chava & Silva-Martinez, 2004).

2.3.3 Compensation fréquentielle de type Miller inverse imbriquée « *Reverse Miller Nested* »

Une autre technique de compensation fréquentielle utilise un étage intermédiaire tampon de type courant « *current buffer* » possédant deux degrés de liberté pour positionner des pôles (résistances en séries) afin d'améliorer la réponse fréquentielle du LDO et ainsi diminuer les « *overshoot* » et « *undershoot* » (Figure 2.10). Bien qu'une très grande efficacité de transmission du courant « *current efficiency* » de l'ordre de 99.95 % est possible, cette approche nécessite une capacité de découplage de l'ordre de 100 nF et utilise une surface de silicium de l'ordre de 0.263 mm^2 en technologie CMOS 0.5 µm. Même en normalisant la technologie à celle souhaitée soit (180 nm), cette approche reste trop volumineuse (0.034 mm^2) (Garimella, Rashid, & Furth, 2010).

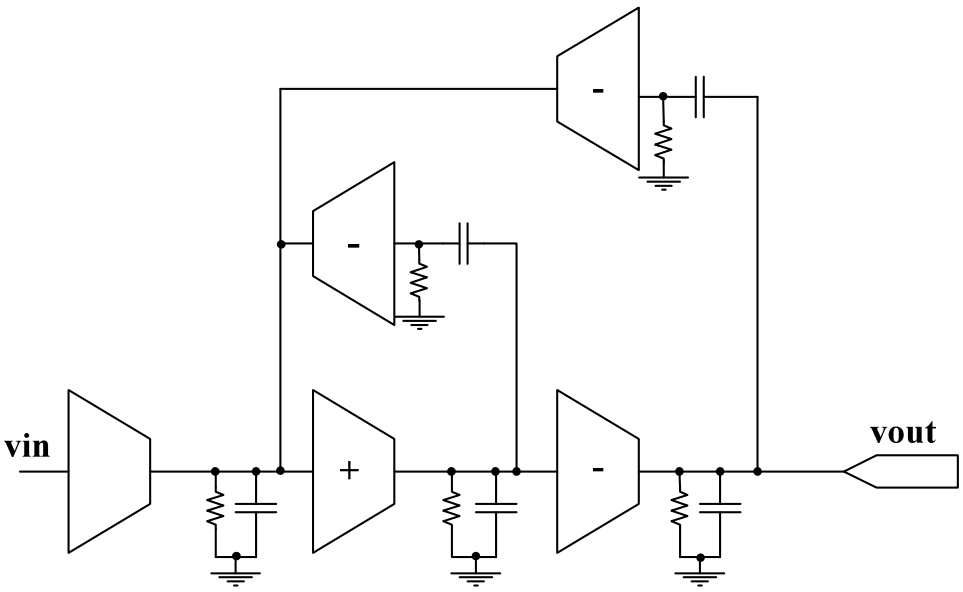


Figure 2.10 LDO à compensation fréquentielle de type Miller inversé imbriqué (Garimella, Rashid, & Furth, 2010).

2.3.4 Compensation fréquentielle par ajout d'un étage tampon

La réponse fréquentielle d'un LDO est dominée par le gain bande-passante de la boucle de rétroaction ainsi que le « *slew-rate* » du transistor de sortie (pMOS de puissance). Ce dernier est souvent de plusieurs milliers de micromètres de largeur créant un nœud capacitif important. Une approche vise à isoler la haute impédance de l'étage d'amplification d'erreur (souvent un amplificateur opérationnel) de l'étage de sortie très capacitive (pMOS de puissance) comme le montre la Figure 2.11. Ceci a pour effet d'améliorer et de stabiliser la boucle de rétroaction du LDO (Leung & Ng, A CMOS low-dropout regulator with momentarily current-boosting voltage buffer, 2010). De plus, la réponse fréquentielle peut être améliorée en augmentant le courant disponible dans la boucle au détriment du courant de fonctionnement « *quiescent current* » (Rincon-Mora & Allen, 1998). Une amélioration possible à l'augmentation directe du courant de polarisation est de détecter le moment où un courant supplémentaire est requis et d'ajuster ce dernier en conséquence (Leung & Ng, A CMOS low-dropout regulator with momentarily current-boosting voltage buffer, 2010) (Al-Shyoukh & Perez, 2007) (Lee, Mok, & Leung, 2005). Ces approches, quoi que très attrayantes, ont le désavantage de devoir utiliser des capacités de découplage et occupent une surface de silicium considérable.

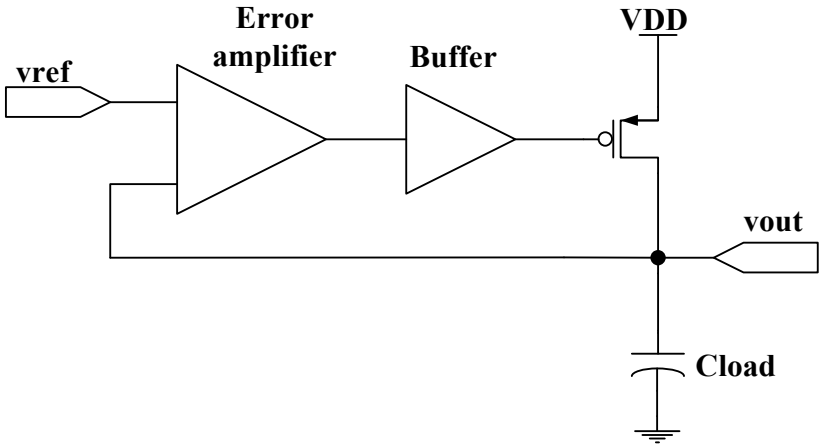


Figure 2.11 Compensation fréquentielle par ajout d'un étage tampon.

Plusieurs variantes de la technique d'ajout d'un étage tampon existent. L'ajout d'une résistance externe en série de 200 mΩ (Figure 2.12) produit un zéro indépendant de la charge active connectée au LDO assurant ainsi un meilleur contrôle sur la boucle de rétroaction (Chen & Wang, 2011). Combinée avec une technique de suralimentation momentanée lors d'une forte demande de courant de la charge, des performances intéressantes peuvent être atteintes. Cependant, une capacité de découplage de l'ordre de 1 µF est nécessaire en plus d'occuper une surface de silicium considérable, soit 415×250 µm en technologie CMOS 180 nm.

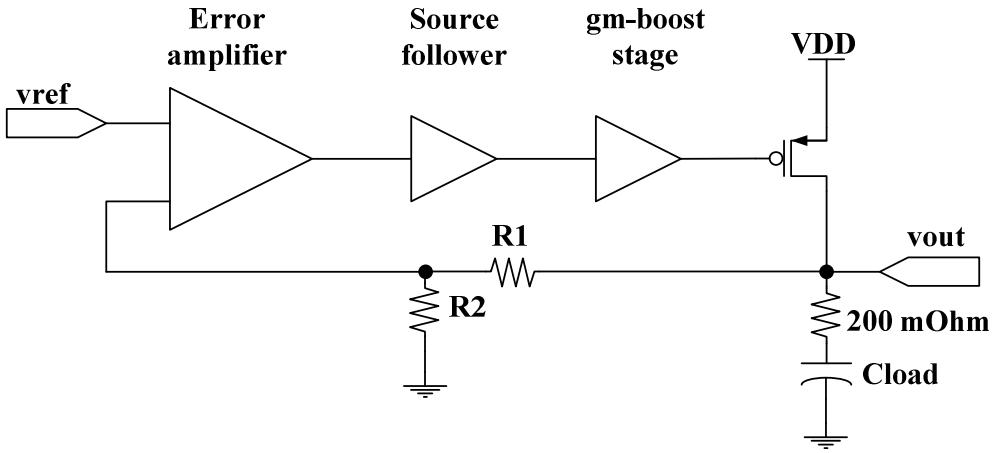


Figure 2.12 LDO avec résistance de sortie en série et suralimentation momentanée (Chen & Wang, 2011)

2.3.5 Compensation fréquentielle par cascade d'étage tampon

L'ajout de plusieurs petits étages tampons entre l'amplificateur d'erreurs et le transistor de puissance (pMOS) a pour but d'améliorer le gain bande-passante de la boucle de rétroaction sans introduire de pôles basses fréquences (Ho, Leung, & Mak, 2010). En cascadant plusieurs étages à faible gain comme le montre la Figure 2.13 on peut obtenir une bonne isolation de l'étage d'amplification d'erreur et de l'étage de puissance de sortie (pMOS) et ainsi conserver une constante de temps RC faible. Une telle approche nécessite néanmoins une capacité de découplage de 1 µF en plus d'occuper une surface de 72.5×37.8 µm en technologie CMOS 90 nm pour un courant maximal de 50 mA.

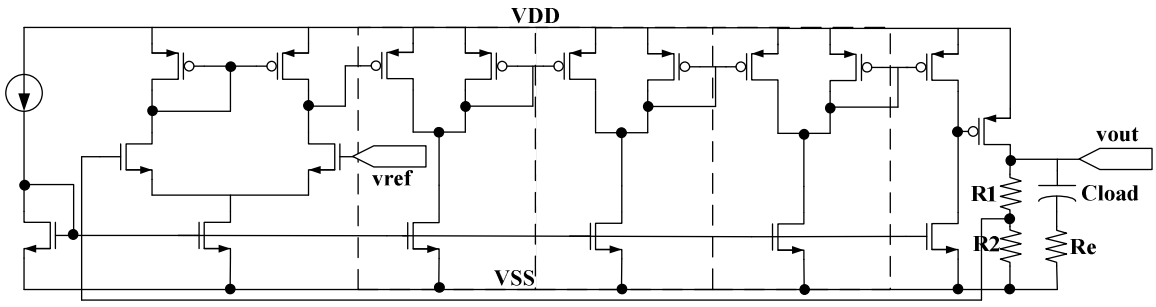


Figure 2.13 Compensation fréquentielle par cascade d'étage tampons (Ho, Leung, & Mak, 2010).

2.3.6 Amplificateur à temps de monté et de descente élevé

Une autre méthode pour améliorer la réponse fréquentielle d'un LDO sans ajouter d'étage tampon est d'améliorer le temps de monté et de descente « *slew-rate* » de l'amplificateur d'erreur. Un amplificateur de type « *push-pull* » où le temps de monté et descente est augmenté améliore le design de base de la Figure 2.8 (Man, Mok, & Chan, 2007) et est montré à la Figure 2.14. Cependant, pour atteindre de bonnes performances, la taille du transistor de puissance de sortie doit être très grande soit environ 6000 µm de large pour une technologie CMOS 180 nm pour un modeste courant maximal de 50 mA.

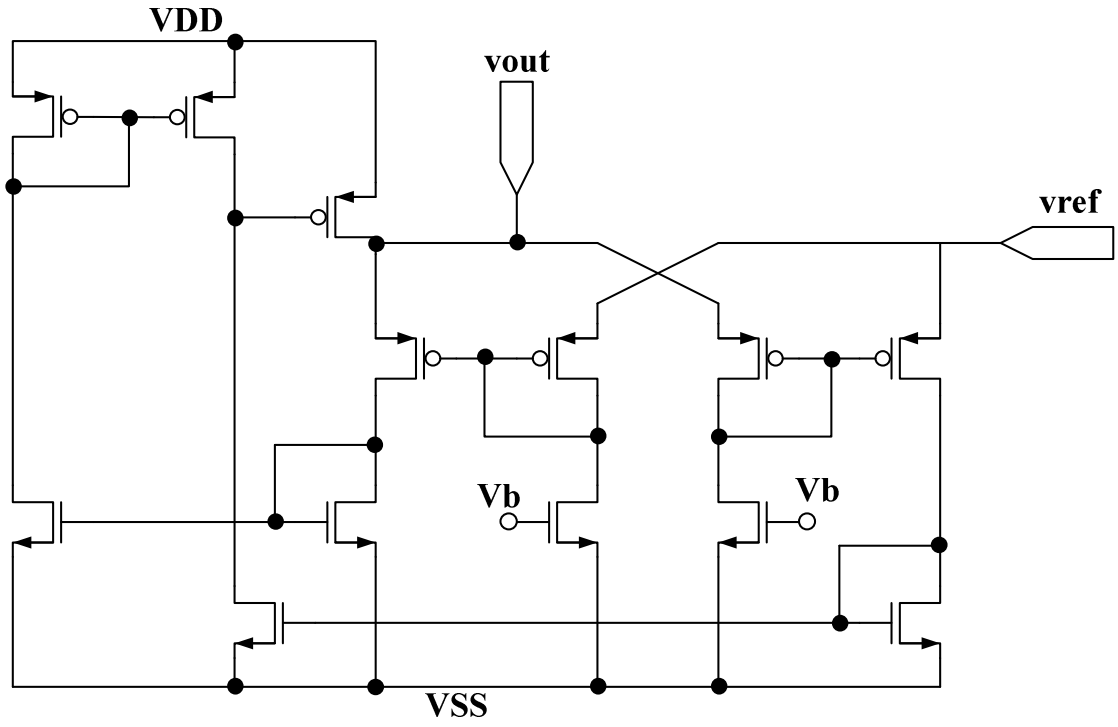


Figure 2.14 LDO avec amplificateur à haut taux de monté et de descente (Man, Mok, & Chan, 2007).

2.3.7 Approche de régulation numérique

Une approche numérique est également envisageable pour la conception de la boucle de rétroaction d'un LDO. Un comparateur fonctionnant à 1 MHz compare la tension de sortie avec la référence (vref) pour produire un signal interprété par un contrôleur numérique qui ajuste l'ouverture ou la fermeture de 256 transistors pMOS de puissance (Figure 2.15). Cette technique permet de réguler une tension de sortie très basse (0.45 V) avec une alimentation principale également très basse (0.5 V). Cependant cette approche ne permet pas un courant de sortie très élevé (200 µA) pour une surface de silicium raisonnable (0.042 mm^2 en technologie CMOS 65 nm) (Okuma, et al., 2010).

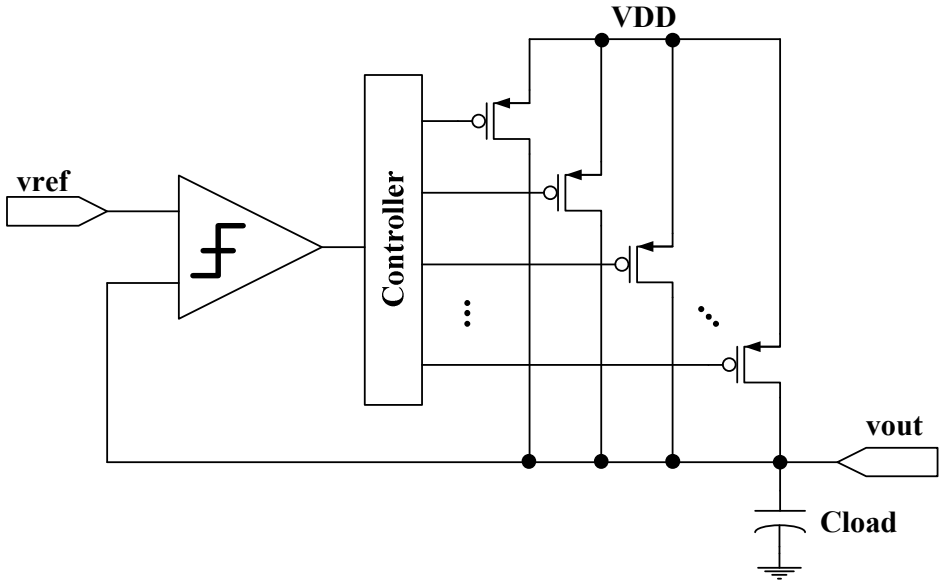


Figure 2.15 LDO avec une boucle de rétroaction numérique (Okuma, et al., 2010).

2.4 Régulateurs linéaires (LDO) sans capacité de découplage externe

L'architecture particulière du WaferIC ne permet pas d'incorporer une capacité de découplage externe afin d'aider la régulation d'une charge active, et ce, pour deux raisons majeures. Aucun lien analogique pur n'existe rendant impossible l'utilisation de capacités de découplage. De plus, puisque les NanoPads ne font qu'environ 100 µm×100 µm, il devient presqu'impossible de déposer manuellement une capacité de découplage connectant exactement le même plot de puissance. Comme la surface de silicium est un enjeu majeur dans ce projet, l'intégration de capacité de découplage dans la tranche n'est pas une option.

Le placement d'une capacité de découplage à la sortie d'un LDO a pour but d'ajouter un pôle à haute fréquence permettant de stabiliser la boucle de rétroaction lorsque la charge active opère à haute fréquence (plusieurs MHz). La capacité agit alors comme réservoir de charges limitant les excursions de tensions positives et négatives « *overshoot/undershoot* » durant un moment afin de permettre à la boucle de rétroactions du LDO de réagir et de fournir le courant supplémentaire ou de le limiter pour conserver une tension de sortie stable (Ho & Mok, 2010).

Un régulateur sans capacité externe a pour avantage d'enlever le pôle dominant à sa sortie régulée. Cela devient possible en faisant des compromis entre la puissance consommée, la

stabilité intrinsèque du régulateur ainsi qu'à son temps de réponse au phénomènes transitoires. Puisque la capacité de sortie n'est plus, les phénomènes transitoires lors des forts appels de courant de la charge ne sont plus absorbés par cette dernière. Le régulateur doit donc avoir un temps de réponse excessivement rapide afin de prévenir une trop grosse chute de la tension régulée de celle-ci. Ce gain en rapidité est souvent atteignable grâce un courant statique et dynamique plus élevé.

2.4.1 Amélioration du temps de monté et descente « *slew-rate* »

Cette technique utilise des étages d'amplification de courant afin de fournir un courant supplémentaire à la boucle de rétroaction contrôlant l'étage de puissance de sortie (pMOS) ou bien, à l'opposée, afin d'offrir un chemin de décharge rapide (Figure 2.16). Cependant, cette technique nécessite l'intégration d'une capacité de découplage intégrée de l'ordre de 7 nF et occupe ainsi une surface de silicium de 0.145 mm^2 pour une technologie CMOS 0.35 µm (Ho & Mok, 2010). D'autres variations existent dans la littérature utilisant une technique semblable (Milliken, Silva-Martinez, & Sanchez-Sinencio, 2007) (Ming, Li, Zhou, & Zhang, 2012).

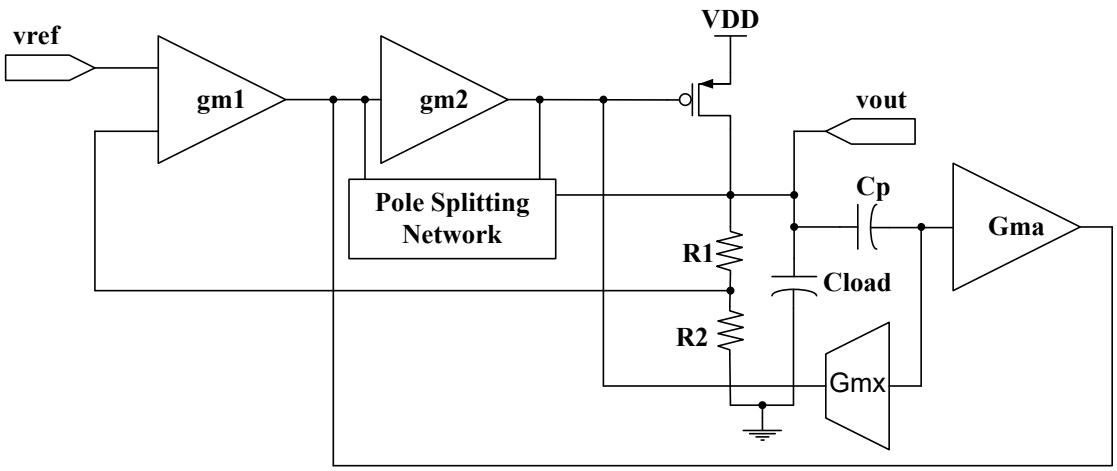


Figure 2.16 LDO sans capacité de découplage par accélération de la boucle de rétroaction en augmentant le « *slew-rate* » (Ho & Mok, 2010).

2.4.2 Détection des excursions de tension de sortie

Une autre technique pour s'affranchir de la capacité de découplage d'un LDO consiste à détecter les excursions de tension positive et négative de la tension de sortie et d'ajuster le courant de polarisation en conséquence afin de diminuer le temps de réponse de la boucle de rétroaction (Figure 2.17). Cette technique permet d'augmenter le courant uniquement lorsque nécessaire permettant ainsi de ne pas détériorer l'efficacité en courant du LDO. Toutefois une capacité de découplage intégrée de 600 pF est nécessaire pour un courant maximal de 66.7 mA pour surface de 587 µm×260 µm en technologie CMOS 0.35 µm(Or & Leung, 2010).

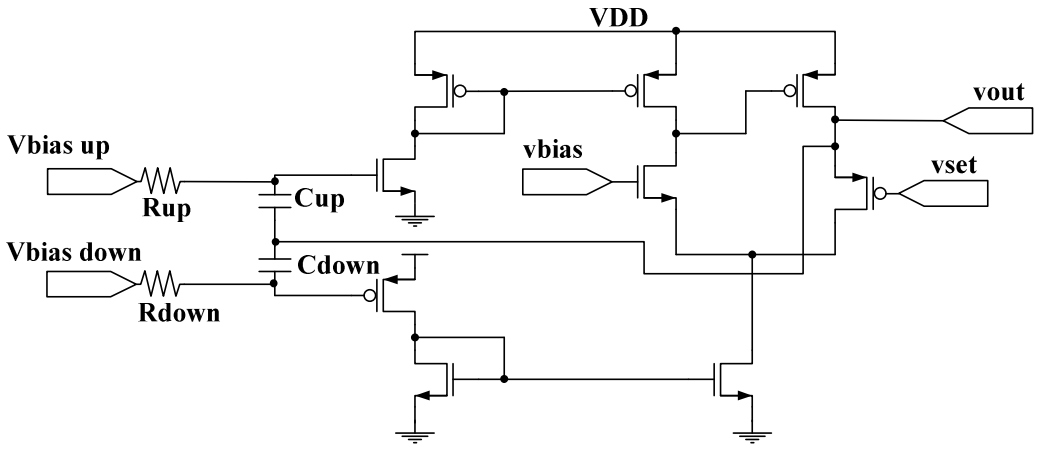


Figure 2.17 LDO sans capacité de découplage par détection des excursions de tension de la sortie (Or & Leung, 2010).

2.4.3 Rétroaction par boucle de courant

Plusieurs approches différentes sont utilisées dans la littérature. (Hazucha, Karnik, Bloechel, Parsons, Finan, & Borkar, 2005) ont introduit en 2005 une technique appelée suiveur de tension inversé (Flip Voltage-Follower) (FVF). L'avantage majeur de cette technique est l'utilisation d'une rétroaction de type "Shunt", ce qui permet de diminuer l'impédance de sortie du transistor de puissance. De cette manière une rétroaction en courant est possible ce qui accélère grandement le temps de réponse d'une telle architecture.

Cette approche permet de découpler la boucle de rétroaction en deux permettant au LDO d'avoir un temps de réponse très rapide (0.54 ns). Or, cette technique intègre une capacité de découplage de 600 pF et occupe une surface de 0.098 mm^2 pour une technologie CMOS 90 nm (Hazucha,

Karnik, Bloechel, Parsons, Finan, & Borkar, 2005). De plus, le courant nécessaire y est beaucoup trop élevé (mA). D'autres travaux dans la littérature utilisent ce concept dans des versions améliorées (Guo & Leung, 2010).

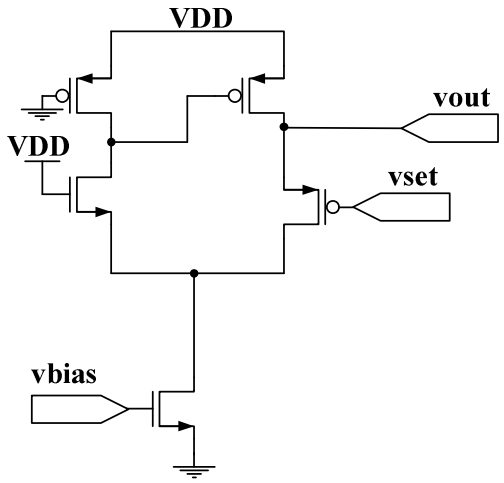


Figure 2.18 LDO sans capacité de découplage par rétroaction en courant (Hazucha, Karnik, Bloechel, Parsons, Finan, & Borkar, 2005).

2.4.4 Approches basées sur le "Flip-Voltage Follower"

D'autres structures du type FVF ont étés détaillés dans la littérature par (X.L TAn, 2014)(Guo & Leung, 2010)(Or & Leung, 2010) ainsi que (T.Y Man, 2008). Chacune des solutions avancées offres des solutions aux problèmes mentionnés précédemment (puissance consommée, surface de silicium). (X.L TAn, 2014) utilisent un schéma de compensation fréquentiel de type Miller à double sommation. Lorsque comparé à une solution basée sur un sommation simple, cette approche offre une meilleure stabilité en déplaçant le pôle dominant vers les hautes fréquences. Cette approche offre un courant maximal de 50 mA pour un courant statique consommé de 23.7 uA et ainsi qu'un temps de réponse de 1.7 us pour une capacité de sortie équivalente entre 10 pF et 10 nF.

Une seconde approche avancée par (Milliken, Silva-Martinez, & Sanchez-Sinencio, 2007) utilise une technique d'amélioration du "slew-rate" combiné à une compensation de Miller simple afin d'améliorer le temps de réponse. La consommation statique de 8 uA est d'un facteur 750x plus faible que le design de référence proposé par (Hazucha, Karnik, Bloechel, Parsons, Finan, &

Borkar, 2005) mais le temps de réponse y est dégradé quant à lui d'un facteur plus de 9000x (5 us en comparaison à 0.54 ns). D'autres solutions sont également proposées afin d'améliorer le temps de réponse du régulateur sans le compromis d'augmentation de la consommation statique. (Or & Leung, 2010) combinent un détecteur de « *peak* » de tension basé sur une cellule de couplage capacitif avec une celle de FVF. La puissance consommée de 19 uA permet un temps de réponse de 3 us. Cependant, cette diminution de 333x de la consommation statique résulte également d'une diminution de performance de 5555x quant au temps de réponse du régulateur. (T.Y Man, 2008) proposent l'ajout d'un simple transistor grille-commune comme transistor de contrôle de grille du transistor de puissance en fonction de la charge. Cette approche est très simple et offre des temps de réponse de l'ordre de 300 ns pour des courant de 50 mA ainsi que pour des capacités de sorties allant de 0 nF jusqu'à 4.7 uF. Cependant le courant statique demandé y est plus important, soit 100 uA. De plus, cette approche est restrictive quant au profil de courant de la charge, seul des sauts de courant spécifiés y sont possible afin de ne pas y dégrader sa stabilité. Plusieurs autres techniques sont documentées dans la littérature tel que de la polarisation dynamique en fonction du courant de la charge, de l'amélioration de « *slew-rate* », de la polarisation de caisson ou des étages de puissances de sorties adaptatifs en fonction du courant demandés. Tous ont leurs mérites et leurs faiblesses.

2.5 Référence de tension

Un des objectifs de ce projet est de pouvoir fournir une grande variété de tensions de références sur une grande plage de valeurs. Ces tensions de références doivent être indépendantes face aux variations de la température, du procédé de fabrication ainsi que des variations de l'alimentation. La littérature regorge de références de type « *Bandgap* » (BGR) offrant d'excellentes performances.

2.5.1 Référence de type bandgap typique

Cette approche utilise, en technologie CMOS, des transistors bipolaires parasites connectés en diodes. Ces derniers offrent une tension qui varie inversement par rapport à la température de manière quasi linéaire. L'équation suivante exprime la tension base-émetteur de cette dernière (Ming, Ma, & Zhang, A high-precision compensated CMOS Bandgap voltage reference withour resistors, 2010).

$$V_{BE}(T) = V_T \ln\left(I_c T^{-\eta} E \exp\frac{V_{G0}}{V_T} \right) \qquad 2.1$$

La Figure 2.19 montre un tel circuit utilisant un amplificateur opérationnel pour maintenir les courants égaux dans les deux branches. D'autres variations existent dans la littérature où l'amplificateur est remplacé par un miroir de courant.

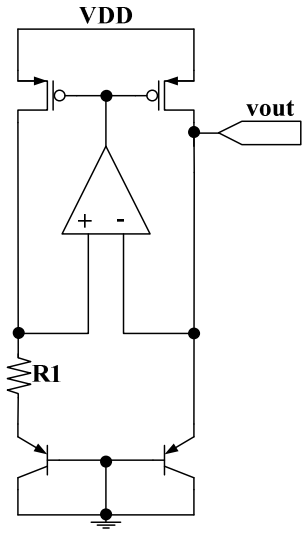


Figure 2.19 Référence de tension de type bandgap utilisant des transistors parasites connectés en diodes (Ming, Ma, & Zhang, A high-precision compensated CMOS Bandgap voltage reference withour resistors, 2010).

2.5.2 Améliorations du circuit typique

Une première amélioration du schéma de base de la Figure 2.19 consiste à ajouter des résistances de type « *poly* » pour générer un courant PTAT qui, une fois combiné à la tension CTAT de la diode parasite donne une tension de sortie très stable face aux variations de la température. La Figure 2.20 montre le circuit et donne des performances très appréciables soit 5.3 ppm/°C face aux variations de la température et 1.43 mV/V face aux variations DC de l'alimentation pour une tension de sortie de 1.4 V. Cependant, cette approche occupe une surface de silicium de 216 µm×256 µm en technologie CMOS 0.6 µm. Même après une normalisation en 0.18 µm cette approche utiliserait plus de 60 % de l'espace disponible d'un NanoPad(Leung, Mok, & Leung, A 2-V 23-uA 5.3-ppm/°C curvature-compensated CMOS bandgap voltage reference, 2003). Une seconde technique propose également l'utilisation de résistances de type « *poly* » (Figure 2.21)

pour atteindre des tensions plus basses de l'ordre de 0.61 V avec une indépendance très grande face à la température (3.9 ppm/°C) (Andreou, Koudounas, & Georgiou, 2012), mais aux dépends de la surface de silicium nécessaire. D'autres approches semblables avec ou sans résistances poly offrent également des performances intéressantes face aux variations de la température, mais utilisent une surface de silicium trop importante (Ming, Ma, & Zhang, A high-precision compensated CMOS Bandgap voltage reference withour resistors, 2010)(Leung & Mok, A sub-1-V 15-ppm/°C CMOS bandgap voltage reference without requiring low threshold voltage device, 2002).

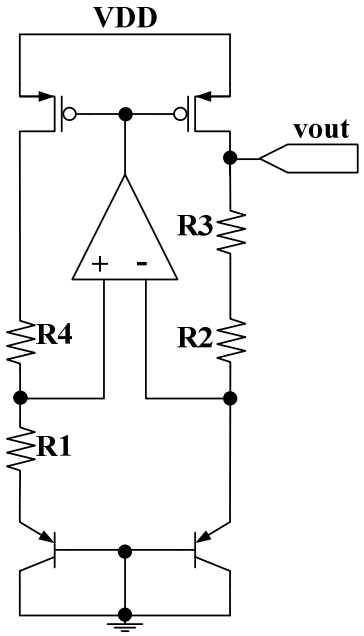


Figure 2.20 Référence de type bandgap utilisant des résistances « *poly* » (Leung, Mok, & Leung, A 2-V 23-uA 5.3-ppm/°C curvature-compensated CMOS bandgap voltage reference, 2003).

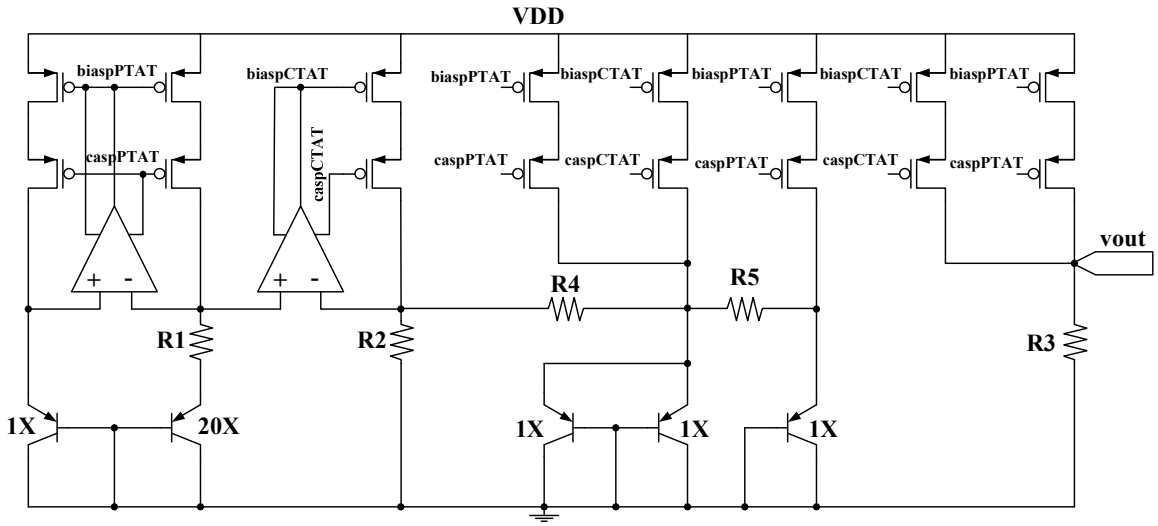


Figure 2.21 Référence de type bandgap utilisant que des résistances « *poly* » (Andreou, Koudounas, & Georgiou, 2012).

2.5.3 Référence de tension sans transistors bipolaires parasites

Puisque les transistors bipolaires parasites ne permettent pas facilement de générer des tensions plus basses que 1.2 V, une approche consiste à utiliser des transistors nMOS connectés en diodes. Cette technique permet d'obtenir des tensions de références plus basses telles que 0.6 V en plus d'occuper une surface de silicium moindre (Ytterdal, 2003) mais demeure plus sensible face aux variations du procédé, puisque ces dernières sont basées sur la tension de seuil V_{th}.

2.6 Référence de tension configurable

2.6.1 Référence de tension configurable avec un diviseur résistif

Une première approche consiste à générer une référence de tension de type bandgap ayant une tension plus élevée (ex : 2.4 V). Cette tension est ensuite dirigée vers un diviseur résistif comme le montre la Figure 2.22. L'approche proposée par (Ramos, Cadeira, & Pimenta, October 2007) dérive une tension de 2.4 V pour la rendre configurable de 0 jusqu'à 2.1 V au travers un diviseur résistif. Un multiplexeur analogique de 3 bits permet donc 8 valeurs différentes de tension de sortie avec une précision de 3 % et une dérive face à la température de 50-100 ppm/°C en technologie CMOS 0.35 µm. D'autres approches semblables sont disponibles dans la littérature

(Khan & Dutta, December 2003) (Ouchen, Hamouda, Wiener, Arnold, Bouguechal, & Manck, May 2006) (Backenius, Sall, Anderson, & Vesterbacka, November 2006).

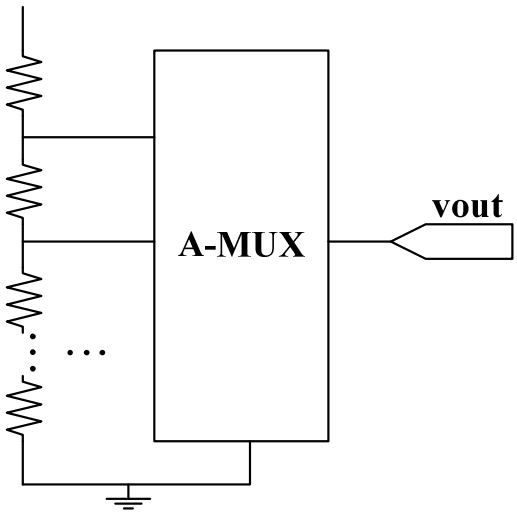


Figure 2.22 Référence de tension configurable à l'aide d'un diviseur résistif et d'un multiplexeur analogique (Ramos, Cadeira, & Pimenta, October 2007).

2.6.2 Référence de tension configurable par changement de ratio de transistors

Une autre approche semblable au diviseur résistif utilise un réseau de transistors et de « *switch* » pour faire varier la taille globale d'un ou de plusieurs transistors pouvant ainsi faire varier le ratio entre transistors ou le courant global qui est forcé dans une branche d'un circuit comme le montre la Figure 2.23. L'approche proposée utilise une référence de tension de type bandgap classique à base de miroir de courant où la valeur de la résistance peut être modulée pour obtenir 32 différentes tensions de sortie. La plage de tension de sortie n'est pas très grande et des pertes de transmissions sont également à prévoir. Cette technique se veut une manière de calibrer et d'ajuster la tension de sortie pour pallier aux variations de procédé (Backenius, Sall, Anderson, & Vesterbacka, November 2006). La littérature propose d'autres architectures basées sur cette approche (Ramasamy, Venkataramani, & Meeenatchisundaram, November 2008) (Dilimot, Brezeanu, Mitu, & Enache, Ocotober 2002) (Zhang, Guo, Kong, & Li, October 2007).

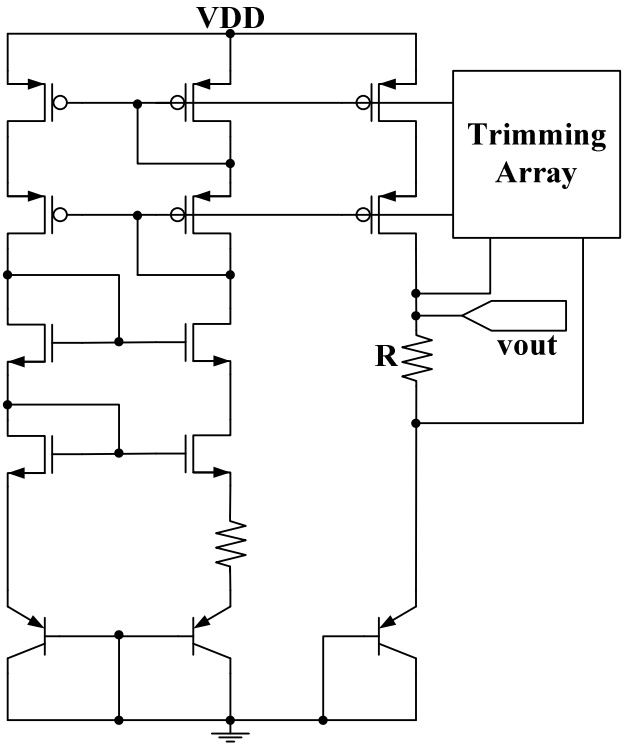


Figure 2.23 Référence de tension configurable par changement de taille de transistors via un réseau de « *switch* » (Backenius, Sall, Anderson, & Vesterbacka, November 2006).

2.6.3 Référence de tension configurable par grille flottante

Cette approche utilise une configuration de grille flottante où la tension de référence est dictée par la différence de charges entre les deux grilles des transistors de la Figure 2.24. En appliquant différentes tensions sur les points d'entrées Vtun, un débalancement est créé forçant le miroir de courant à rétablir un courant identique dans les deux branches et faisant ainsi varier la tension de sortie. On peut obtenir des tensions de sortie variant de 50 mV jusqu'à 0.6 V avec une précision de 40 µV (Srinivasan, Serrano, Twigg, & Hasler, 2008). De plus cette technique est compacte : elle n'occupe que 52 µm×42 µm pour une technologie CMOS 0.35 µm. Par contre, la plage de tension de sortie est plutôt faible et nécessite des tensions Vtun configurables.

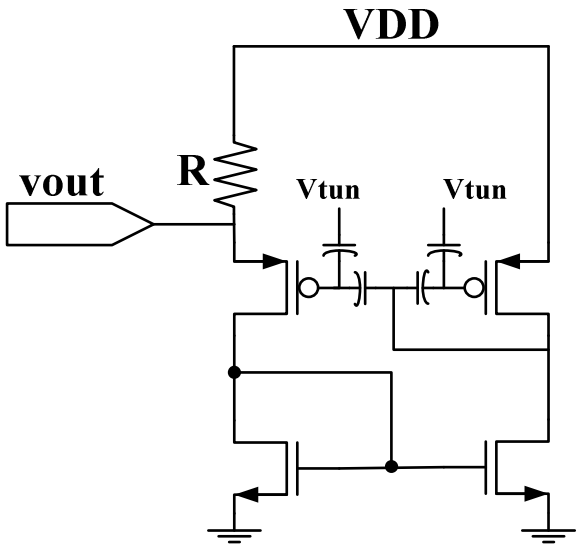


Figure 2.24 Référence de tension configurable par grille flottante (Srinivasan, Serrano, Twigg, & Hasler, 2008).

2.6.4 Référence de tension configurable par approche numérique

Une autre approche utilise un microcontrôleur qui module une tension de référence de type bandgap générée de manière classique. En modulant cette tension par un « Pulse Width Modulator » (PWD) dans un modulateur sigma-delta de premier ordre et en filtrant la sortie à l'aide d'un filtre passe bas passif (Figure 2.25), on peut obtenir des tensions de sortie variant de 0 à 2.5 V avec 10 bits de précision et une faible dérive par rapport à la température de l'ordre de 100 ppm/°C (Kennedy & Rinne, June 2005).

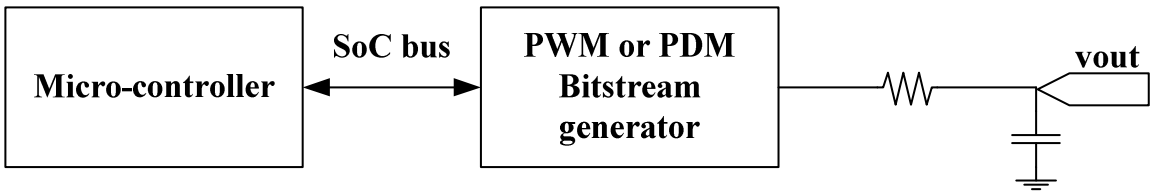


Figure 2.25 Référence de tension configurable employant une approche numérique (Kennedy & Rinne, June 2005).

2.7 Convertisseur Analogique Numérique (CAN)

Il existe 4 grandes familles de convertisseurs analogique-numérique : le type pipeline « *pipeline* », le type instantané « *flash* », le type par approximations successives « *successive approximation* » et le type par sur-échantillonnage « *oversampling* » (Walden, 1999). Ils y seront ici détaillés avec leurs forces et leurs faiblesses. Une revue plus approfondie du type « *successive approximation* » sera ensuite effectuée.

2.7.1 CAN de type « *Flash* »

Ce type de convertisseur est généralement le plus rapide. Il utilise 2^n-1 comparateurs et 2^n résistances ou n est le nombre de bits du convertisseur. Une comparaison parallèle est effectuée avec la tension d'entrée Vin et toutes les tensions de références générées (Figure 2.26). Il en résulte un mot binaire avec un encodage de type thermomètre « *thermometer coding* ». Ce type d'architecture nécessite plusieurs résistances et comparateurs en plus d'être souvent limité à 8 bits de précision pour des raisons de surface de silicium. Chaque bit ajouté à la surface double. Donc, pour un CAN de 8 bits il en résulte 255 comparateurs et 256 résistances (CMOS Design, Layout and Simulation, Second Edition, 2007), (Yang, Naing, & Brodersen, 2010).

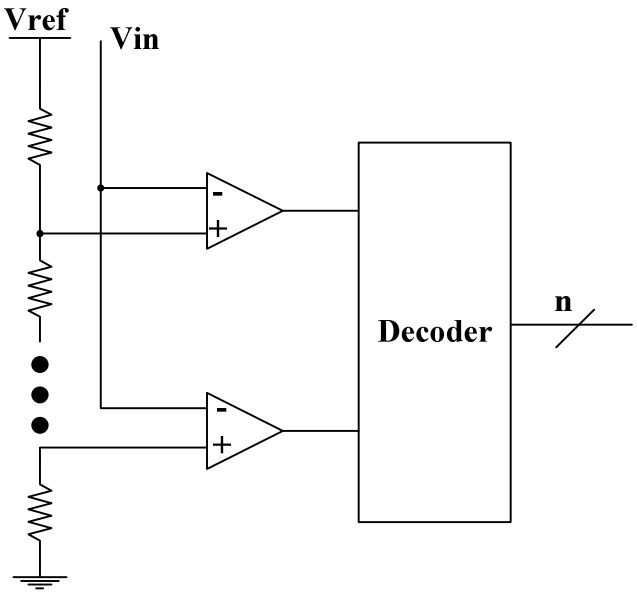


Figure 2.26 Convertisseur analogique numérique de type « *flash* ».

2.7.2 CAN de type « *Pipeline* »

Le convertisseur de type pipeline utilise n étages de conversion du type de la Figure 2.27. L'entrée est échantillonnée par un circuit de « *sample and hold* » (S/H) et est comparée avec une tension de référence Vref/2. Dans le cas où la tension d'entrée est plus grande que Vref/2, la sortie du comparateur affichera un '1' logique. Vref/2 est ensuite soustrait du signal échantillonné et est envoyé à l'amplificateur x2. Si le résultat de la comparaison est un '0' logique, la valeur initiale est passée à l'étage suivant et non la valeur soustraite de Vref/2. Puis, l'opération recommence à l'étage suivant. Ce type de convertisseur permet d'atteindre une haute résolution (10-13 bits) avec une vitesse relativement rapide (CMOS Design, Layout and Simulation, Second Edition, 2007), (Jiang, Do, Yeo, & Lim, 2008).

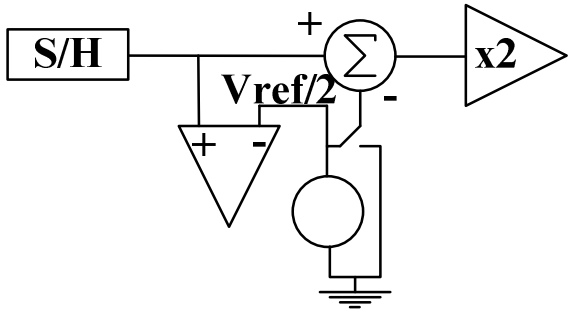


Figure 2.27 Cellule d'un CAN de type pipeline.

2.7.3 CAN de type « *Successive approximation* »

Le convertisseur de type « *successive approximation* » effectue une recherche binaire de la tension Vin en la comparant à une tension générée par un CNA. Lorsqu'une recherche est fructueuse le mot binaire de n bits est alors obtenu (value) comme le montre la Figure 2.28. Ce type de convertisseur est l'un des plus utilisé, car il permet d'obtenir de très hautes résolutions et est rapide tout en demeurant petit et simple (CMOS Design, Layout and Simulation, Second Edition, 2007), (Yang, Naing, & Brodersen, 2010), (Huang, Liu, Lin, & Chang, 2009), (Lotfi, Majidi, Maymandi-Nejad, & Serdijn, 2009).

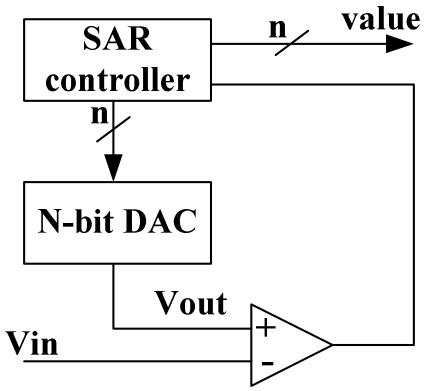


Figure 2.28 CAN de type « *successive approximation* »

2.7.4 CAN de type « *Oversampling* »

Ce type de convertisseur échantillonne le signal désiré à une fréquence bien plus élevée que le critère de Nyquist (f_N =2F où F est la bande passante du signal). Ce type de convertisseur permet d'atteindre de hautes résolutions puisque des techniques de conditionnement de signaux numériques sont utilisées plutôt que des blocs analogiques purs qui nécessitent une attention particulière et qui sont plus difficiles à concevoir. La Figure 2.29 montre le schéma bloc de ce type de convertisseur. Un des avantages de ce type de CAN est que le phénomène « *d'aliasing* » ne devient plus un facteur important contrairement aux autres types de convertisseur qui utilisent des circuits de « *sample and hold* ». Ils utilisent généralement une architecture de capacités commutées « *switched-capacitor* ». Ce type de convertisseur est donc très précis et rapide, mais est plus complexe à réaliser en plus d'occuper une surface plus grande que le type « *successive approximation* » (CMOS Design, Layout and Simulation, Second Edition, 2007), (Dorrer, Greco, Torta, & Hartig, 2005).

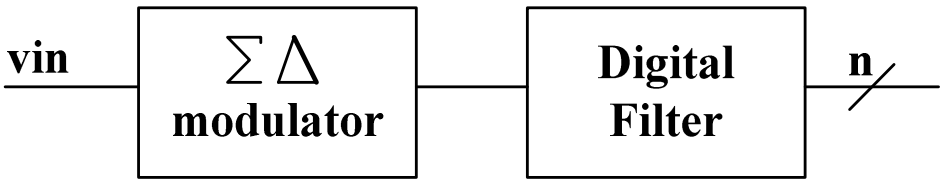


Figure 2.29 CAN de type « *oversampling* »

2.7.5 Résumé

Après l'examen des diverses topologies existantes de convertisseurs analogique numérique, une seule approche permet une intégration à grande échelle pour le WaferIC. L'espace restreint en termes de surface de silicium ne permet pas l'intégration d'un grand nombre de résistances, de capacités, de comparateurs, d'amplificateurs ou de composantes numériques complexes. Les types « *flash* », « *pipeline* » et « *oversampling* » ne sont donc pas des approches adéquates pour obtenir une surface de silicium compacte. L'approche « *successive approximation* » offre une avenue possible pour sa simplicité et sa taille.

2.7.6 Revue Approfondie « *SAR-ADC* »

Le CAN de type « *SAR-ADC* » offre des résolutions plus grandes avec le compromis d'une vitesse de conversion réduite puisqu'une conversion du domaine analogique vers le domaine numérique nécessite plusieurs cycles d'horloge et de comparaisons avec une tension de référence générée par un CNA (Yang, Naing, & Brodersen, 2010). Tous les types de convertisseurs « *SAR-ADC* » ont en commun trois blocs distincts, tel que discuté à la section 2.7.3. Les différences majeures se retrouvent dans le module CNA, alors que le comparateur avec le « *sample & hold* » ainsi que le module de contrôle numérique sont très fortement semblables. La surface de silicium et les performances du « *SAR-ADC* » dépendent donc du choix et de l'implémentation du CNA. La méthode « *switched capacitor* » (Yang, Naing, & Brodersen, 2010), (Huang, Liu, Lin, & Chang, 2009), (Lotfi, Majidi, Maymandi-Nejad, & Serdijn, 2009), (Shin & Kwon, 2011), (Cho, Jeon, Nam, & Kwon, 2010)est la technique de prédilection pour les applications à faible consommation de courant en comparaison avec la méthode de type « *current steering* ».

La littérature regorge de « *SAR-ADC* » où la vitesse d'échantillonnage, la surface de silicium ainsi que la consommation de courant sont les objectifs premiers des concepteurs. Afin de diminuer le temps de conversion, plusieurs techniques existent telles que l'utilisation d'un procédé asynchrone, ce qui permet aux auteurs de (Yang, Naing, & Brodersen, 2010) d'atteindre un taux de conversion de 1GS/s pour une conversion de 6-bits avec une consommation de 6.7mW et une surface de silicium de $0.11mm^2$ pour une technologie de CMOS de 65nm. Une autre technique utilise une variance du « *SAR-ADC* » soit la méthode d'approximation successive ternaire ou « *TSAR-ADC* ». Cette méthode examine l'information transitoire d'un « *SAR-ADC* » typique pour en améliorer la précision, la vitesse et la consommation de courant. Un « *TSAR-*

ADC » d'une résolution de 10-bits pour une consommation de 84µW à 8MHz avec une technologie 0.13µm dans une surface de silicium de 0.056mm^2 est reporté par les auteurs de (Guerber, Venkatram, Gande, Waters, & Moon, 2012). Plusieurs autres designs et techniques permettent d'amoindrir la consommation de courant et la surface et sont reportés dans (Huang, Liu, Lin, & Chang, 2009), (Cho, Jeon, Nam, & Kwon, 2010), (Huang, Chang, Liu, & Lin, 2012), (Lin, Liu, Huang, Shyu, Liu, & Chang, 2013), (Hu, Liu, Nguyen, Lie, & Ginsburg, 2013), (Xu, Liu, & Yuan, 2012). Cependant aucune architecture connue ou répertoriée ne permet une intégration dans la surface semblable de silicium à celle d'un CPAD (0.008mm^2).

2.8 Convertisseur Numérique Analogique (CNA)

Il existe une très grande variété de CNA. Ils peuvent être très complexes où très simples allant d'une simple division résistive, à la technique de sommation de courant « *current steering* » en passant par l'adaptation de charge « *charge scaling* ». Tous viennent avec leur lot d'avantages et d'inconvénients mais ont tous un point en commun, un « *matching* » très serré du « *layout* » (CMOS Design, Layout and Simulation, Second Edition, 2007).

2.8.1 CNA de type diviseur résistif

Ce type de CNA s'apparente beaucoup au CAN de type « flash ». Ils utilisent un réseau de résistances et d'interrupteurs combiné à une tension de référence de type « *bandgap* ». Cette tension de référence est divisée et un mot binaire sélectionne le bon nœud résistif pour en extraire la tension de sortie. Cette technique, quoique simple, est très coûteuse en surface de silicium et double pratiquement à chaque bit ajouté (CMOS Design, Layout and Simulation, Second Edition, 2007), (Wei, et al., 2012), (Verma & Razavi, 2009), (Seo, 2008).

2.8.2 CNA de type « *current steering* »

Cette technique utilise des sources de courant très précises qui peuvent être additionnées entre elles pour un courant total correspondant au mot binaire désiré. Cette technique utilise un mot binaire de type thermomètre « *thermometer encoding* » et ajoute une valeur préétablie de courant à chaque bit supplémentaire. Le courant est ensuite converti en tension de sortie (Tseng, Fan, & Wu, 2011). Cette technique requiert un nombre important de sources de courant qui doivent être identiques rendant le « *layout* » plus ardu et plus volumineux (CMOS Design, Layout and

Simulation, Second Edition, 2007), (Tseng, Fan, & Wu, 2011), (Kim, Jeon, Lee, Yang, Ryu, & Cho, 2011).

2.8.3 CNA de type « *current steering binary weighted* »

Cette technique reprend l'idée de base des CNA de type « *current steering* » en ajoutant une dimension supplémentaire soit le poids du courant. Une croissance binaire du courant (1, 2, 4, 8) permet un plus grand éventail de courants, donc de tensions de sortie tout en demeurant compact et en utilisant moins de bits de configuration. Cette technique requiert également un grand nombre de sources de courant identiques et volumineuses (CMOS Design, Layout and Simulation, Second Edition, 2007), (Tiilikainen, 2001), (Lin & Kuo, A compact dynamic-performance-improved current-steering DAC with random rotation-based binary-weighted selection, 2012), (Seo, 2008), (Deveugele & Steyaert, 2006), (Wu, Palmers, & Steyaert, 2008), (Zaki, et al., 2012).

2.8.4 CNA de type « *charge scaling* »

Cette technique utilise un réseau de capacités commutées pouvant être chargées ou déchargées faisant ainsi varier la charge total d'un système. Combinée avec une tension de référence stable cette technique permet d'obtenir une tension de sortie qui est une fonction de la distribution de la charge sur les capacités connectées. Cette technique est très populaire mais nécessite l'intégration d'un grand nombre de capacités, soit 2^N (CMOS Design, Layout and Simulation, Second Edition, 2007), (Hu, Liu, Nguyen, Lie, & Ginsburg, 2013), (J.Bell, 2005), (Paulino, Franca, & Martins, 1995), (Lee & Lee, 2010), (Jeon, et al., 2009).

2.8.5 Résumé

Cette revue de littérature confirme qu'il est nécessaire d'effectuer les présentes recherches et de développer une nouvelle approche afin de distribuer de la puissance et d'interfacer des signaux numériques et analogiques pour le WaferIC. Il n'existe aucune solution viable dans l'état de l'art permettant de répondre aux besoins présents tout en étant possible de les intégrer dans la surface de silicium très restreinte.

2.9 Conclusion de la revue de littérature

Ce chapitre a été l'objet d'une étude approfondie sur la structure particulière du WaferIC ainsi que des contraintes qu'ils y sont associées. Il en émane que la surface de silicium est la problématique la plus criante avec une surface par Cellule de 0.3136 mm^2 et de 0.00847 mm^2 par CPAD. Chaque CPAD doit être en mesure d'accéder à toutes les fonctionnalités lui permettant de s'interfacer avec n'importe quel type de bille qui pourrait s'y interfacer : fournir une tension régulée variant entre 0 et 3.3 V en tenant compte des effets thermiques d'une régulation à bas voltage (ex : 1.0 V) sans l'utilisation de capacité externe de découplage, fournir un plot d'E/S numérique et analogique permettant de propager n'importe quel signal dans tout le WaferIC. Il n'existe aucune solution connue dans la littérature qui permet de réunir toutes les conditions nécessaires à la conception du WaferIC, spécialement en ce qui attrait à la surface de silicium compacte nécessaire. De nouvelles avenues doivent être explorées.

CHAPITRE 3 AMÉLIORATION DE LA DISSIPATION THERMIQUE DE LA RÉGULATION PAR L'AJOUT D'UNE SECONDE RAIL D'ALIMENTATION

3.1 Résumé

Tel que discuté dans les sections précédentes, la version préliminaire du WaferIC n'utilise qu'un rail d'alimentation de 3.3 V pour réguler la charge qui serait déposée sur un NanoPad. Ceci mène à une problématique de dissipation de chaleur trop importante lorsqu'une charge à basse tension (ex : 1.0 V) doit être régulée, où l'efficacité du régulateur chute drastiquement à moins de 30 % (efficacité $\approx V_{OUT}/V_{IN}$). Cela signifie qu'un processeur déposé à la surface du WaferIC et requérant une puissance de 50 W nécessiterait du WaferIC une puissance dissipée de plus de 116 W sous forme de chaleur. De plus, l'alimentation des circuits intégrés tend à s'effectuer à basse tension, requérant plus de puissance, tandis que l'alimentation des plots de sortie s'effectue à plus haut voltage, requérant une puissance modérée à faible.

Dans l'optique de « *wafer-scale* », l'utilisation de régulateur linéaire est un choix qui s'impose de par son absence de composantes passives telles que des inductances ou capacités en comparaison avec les régulateurs de type « *switching* ». Dans cet optique, une solution utilisant des régulateurs linéaires intégrés, nécessite un rail d'alimentation à plus basse tension afin d'améliorer le rendement énergétique de celui-ci lorsqu'une régulation à faible voltage est requise.

L'article « *A Configurable Multi-Rail Power and I/O Pad Applied to Wafer-Scale Systems* » a été publié à la revue de journal « *IEEE Transactions on Circuits and Systems I : Regular Papers* » en novembre 2014. Cet article présente une nouvelle architecture à multi-rail d'alimentation combiné avec un plot d'E/S numérique configurable de 500 mV jusqu'à 2.995 V. Une puce d'essai a été fabriquée et testées en technologie CMOS 0.18 µm dans une surface de 0.008 mm^2 et y inclut une version à deux rails, 1.8 et 3.3 V. Le régulateur linéaire proposé utilise une technique où les boucles de rétroaction et de contrôle sont communes pour les deux rails, le tout à l'aide d'une architecture configurable de transistors communs. La régulation peut fournir un courant maximal de 40 mA avec un temps de réponse de 21.1 ns, une rejection du bruit de l'alimentation jusqu'à 40 dB et peut être mis hors tension pour un courant de fuite total de

145 nA. Le plot d'E/S fonctionne en parallèle avec le régulateur et peut atteindre une vitesse maximale de 250 MHz.

3.2 Contribution au domaine scientifique

La contribution majeure de cet article est la proposition d'une architecture nouvelle d'un régulateur linéaire ne nécessitant aucune capacité de découplage et pouvant être adapté à plusieurs rails d'alimentation le tout dans une surface de silicium ultra compacte de 0.008 mm^2 et utilisant une topologie configurable de partage de transistors ce qui contribue à l'obtention d'une surface de silicium minime. La contribution majeure de cet article, en comparaison avec la littérature, est que ce régulateur linéaire sans capacité de découplage et offrant deux rails d'alimentation offrent des performances équivalentes mais dans une surface de silicium beaucoup moindre.

Une erreur s'est introduite par rapport au terme utilisé tout au long de l'article et faisant référence à un « *Fast Load Regulator* » (FLR). L'utilisation de ce terme est erronée dans l'article, on devrait simplement avoir utilisé le terme « *Linear Regulator* » ou bien « *Low-Dropout Regulator* ».

3.3 Article #1 : A Configurable Multi-Rail Power and I/O Pad Applied to Wafer-Scale Systems

***Abstract*—**We proposes in this paper a novel configurable multi-power-rail pad that combines power supply support circuits and a digital input/output (I/O) buffers designed for a wafer-scale system. This wafer-scale platform includes a reconfigurable wafer-scale circuit, the WaferIC, comprising an alignment-insensitive surface that can be configured to interconnect any digital components manually deposited on its surface. The proposed multi-power-rail pad minimizes power losses and heat dissipation within the circuit. The pad that is fed from two distinct voltage sources providing power at 1.8 and 3.3 V has been implemented and tested. This pad has two merged configurable control loops that can select the power source. Merging takes place through shared transistors. This dual supply pad embeds a voltage regulator that achieves a fast response time of 21.1 ns and that can operate over a wide range of configurable regulated output voltage, from 500 mV up to 2.955 V. This regulator is capable of providing a maximum output current of 40 mA while needing only a very small quiescent current of 126 µA. The regulator's power supply noise rejection ranges from -25 down to -40 dB for frequencies ranging from 1 kHz up to 1 MHz. The embedded digital I/O pad shares a common output with the power distribution and can be configured from 0.5 up to 3.3 V for a maximum speed of 250 MHz.

3.3.1 INTRODUCTION

TODAY'S electronic systems are constantly growing in size and complexity. The increasing complexity combined with decreasing time to market makes it challenging for designers to meet cost and performance constraints.

A novel electronic system prototyping platform has been recently introduced to address these issues [1]–[3]. This platform is based on an active surface implemented using a 200 mm full wafer device. This active surface is covered with over 1.2 million tiny conductive pads called NanoPads interconnected with a configurable interconnection networks. Every Unit-Cell comprises a 4×4 array of NanoPads, and a 32×32 array of Unit-Cells defines a reticle image. The assembly at wafer-scale level is called WaferIC^{TM} and is achieved by photo-repeating 76 copies of the reticle image that are stitched together to implement wafer scale interconnections [3].

When using the prototyping platform, user integrated circuits (uICs) are deposited on the active surface to build the target electronic system. This surface is designed to be insensitive to the alignment of deposited uICs (Figure 3.1a). A thermal flexible pouch, filled with a thermal grease to evacuate heat, is put on top of the uICs firmly held in place by a uniformly applied pressure to ensure good electrical contact, with an anisotropic conductive film (Z-axis film) that embeds conductive vertical fibers (nickel needles) [4]. The Z-axis film also protects NanoPads from possible mechanical damage (Figure 3.1b). A short-circuit detection mechanism maps all the uIC balls connected to more than one NanoPad, and the platform allows creating all the connections specified by a user netlist (Figure 3.1c).

The active surface must also feed power to the uICs. This is done from the bottom of the WaferIC using Through Silicon Vias (TSVs) for adequate signal integrity [3]. The top side of the WaferIC must be free of any other mechanical or electrical structures to ensure good electrical contact between uICs balls and the Z-axis film wires, which means that no decoupling capacitor or external components can be used on the WaferIC. The digital interconnection between two or more distant NanoPads is accomplished by the WaferNet^{TM}. This WaferNet is a very dense configurable interconnection network that spreads between Unit-Cells in every direction (N-S-E-W) with unidirectional connections of various lengths. These connections have lengths 2, 4, 8, 16

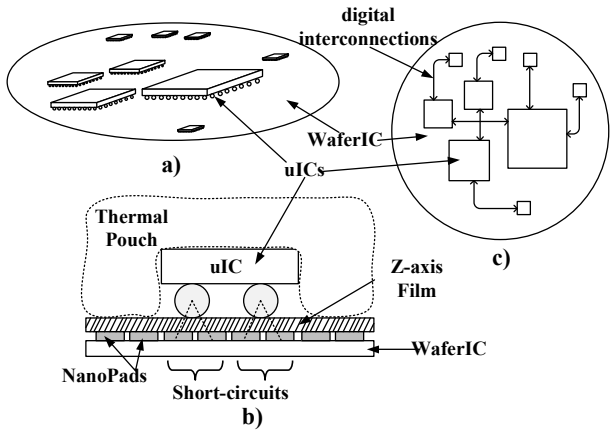


Figure 3.1 (a) WaferIC with user integrated circuits (uICs) deposited on its alignment insensitive surface. (b) Platform cross-section where pressure in the thermal pouch ensures good electrical contact between uIC balls and the NanoPads through a Z-axis film. (c) Interconnection of uICs through the WaferNet.

and 32, where for instance 8 means that the connected Unit-Cells are separated by 7 others [1].

The WaferIC needs to accommodate any type of uIC such as FPGAs, processors, SRAM and DDR memories resulting in a wide range of power supply requirements. For instance, a powerful processor (of size 40×40 mm^2) can requires 60 W [5] (an X86 device is used for reference) to correctly operate, causing intense heating if that power is fed to a 1.2 V device from a 3.3 V supply. In that case the theoretical efficiency would at best be 36%, with 165 W drawn from the power source, 60 W fed to the uIC, and 105 W lost due to joule heating in the embedded regulator. Thermal analysis shown that with adequate air flow and heat transfer the wafer can handle a maximum of 40 W of heat dissipation in the 40×40 mm^2 area occupied by the device package (for a 0.0016 mm^2 uIC), excluding the power absorbed by the uIC, for a total of 100 W or 62.5 mW/mm^2 [5]. This thermal constraint sets at 60 % the minimum required theoretical efficiency of the embedded regulator [3]. With that target efficiency, the embedded regulators should not use the 3.3 V supply to feed large amounts of power to the uIC at supply voltages below 2.0 V. This paper proposes a means to minimize thermal losses of distributed embedded linear regulators by feeding them from multiple power rails.

The following section describes the WaferIC and the constraints associated with its architectures. It also provides an overview of an existing solution for the embedded regulators for the NanoPads. Section III proposes a transistor level architecture for a configurable pad that can serve as an input, an output, or a power supply, and that can draw power from multiple power rails. The pad embeds a novel fast regulator that takes advantage of several power supply sources in order to improve power efficiency when providing power at low voltages as well as a configurable digital I/O. Section IV gives the experimental results measured from a testchip exploiting the proposed architecture that was implemented using the TSMC 0.18 µm CMOS technology. These results demonstrate the benefits of the proposed topology. Experimental results are detailed, discussed and compared with other published works.

3.3.2 WaferIC Description and Existing Solutions

3.3.2.1 The WaferIC

A structural view of two WaferIC's Unit-Cells is shown in Figure 3.2, where 54 % (hatched area) of the silicon area is dedicated to digital circuits such as the WaferNet and the JTAG circuitries

Tableau 3.1 Summary of the NanoPad (NP), Unit-Cell (UC), Reticle Image (RI) and WaferIC (WIC) voltage output capabilities and physical characteristics and requirements.

	Number	**Max Current**	**Output levels**	**Area (mm^2)**
NanoPad (NP)	16/UC	>50 mA	0.0 to 3.3 V	0.00847
Unit-Cell (UC)	1024/RI	>100 mA	-	0.3136
Reticle Image (RI)	76/WIC	5A	-	321.1264
WaferIC (WIC)	-	380 A	-	24405

used to configure the WaferIC. The remaining 46 % area is for NanoPads. Each NanoPad can be configured as a ground, a power supply providing up to 3.3 V, a configurable digital output compatible with voltage supplies ranging from 0.5 V up to 3.3 V, a CMOS digital input or an open circuit (high impedance) [3]. The silicon area is one of the most important issues for the WaferIC closely followed by the quiescent current. Tableau 3.1 lists the foremost objectives and constraints regarding the WaferIC output capabilities and physical restraints.

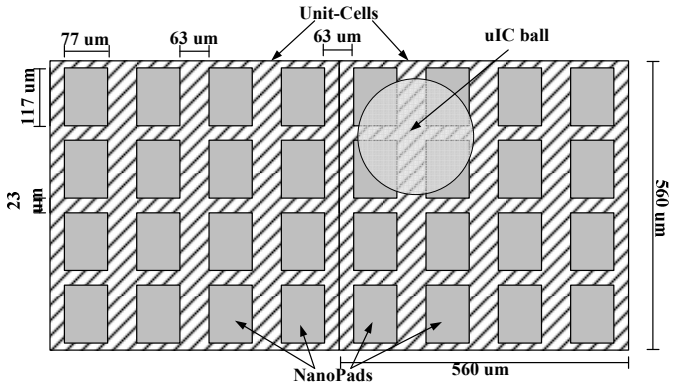


Figure 3.2 Unit-Cell and NanoPad sizes where the hatched area is dedicated to digital circuits and WaferIC configuration and the grey area to the NanoPads

Switching regulators can attain very high power efficiencies of up to 95%, which would result in a power saving over 35 W for the example depicted earlier (60 W processor) [6]. However, such regulators typically require external passive components making them very hard to integrate in limited silicon area (Tableau 3.1). As a fully integrated solution is required for the WaferIC, the switching regulator approach is not possible.

For a given output voltage, the efficiency of linear regulator directly depends on its power supply voltage. Lowering the 3.3 V power rail can be a suitable solution to improve power efficiency, as long as the circuitry itself still operates adequately. However, a lower power supply voltage reduces the maximum regulated output voltage. Moreover, the power distribution structure described in [3] offers limited possibilities to adjust the source supply voltage, since the power rails supply several thousand NanoPads, connected to different uICs with possibly different power supply requirements. In [3], the whole WaferIC is powered by 1.8 V and 3.3 V rails. The 1.8 V rail is dedicated to the cell logic core (WaferNet and JTAG), and the 3.3 V rail supplies power to all other analog circuits (e.g. NanoPads). Several reticle images (up to 4) are externally fed by a same voltage source. Considering the multiple simultaneous requirements, lowering the supply voltages to increase efficiency is not an option, since many other analog circuits or NanoPads obtaining their voltage power from a same electrical node need the full scale voltage of the power rail to operate correctly.

3.3.2.2 Single Rail Configurable Power I/O PAD

The design proposed in [3] takes advantage of a hierarchical topology derived from [7] in order to minimize quiescent current and silicon area consumption by sharing the maximum number of common circuitries. A master-slave topology is used in every Unit-Cell. In reference to Figure 3.3(a), the top module uses a reference voltage (V_{SET}) shared between 16 NanoPads. The Fast Load Regulator (FLR) embedded in each NanoPad (Figure 3.3b) uses V_{SET} to set the output voltage within the range of 1.0 V to 2.5 V. In addition, V_{SET} sets the digital I/O voltage levels. This technique leads to a reduction in silicon area by sharing the fast load regulator with the digital I/O to provide power through configurable voltage (V_{SET}), which avoids duplicating power stages for supplying the digital I/O. However, control circuits must be added to share this regulated power supply between the digital I/O and the load. This comes at the cost of speed for

both the I/O and the FLR response time, since the pass transistor loads the digital output (large transistor) and a significant parasitic capacitance is added by its gate.

The configurable I/O pad proposed in [3] (Figure 3.3) integrates a digital I/O within the regulation loop coupled with a boost technique using a differential pair. This digital I/O can be configured to fit standard CMOS voltages of 1.0, 1.2, 1.5, 1.8, 2.0, 2.5 and 3.3 V with a post-layout simulated bandwidth of over 300 MHz with a 5 pF load. This approach allows very high current capabilities within a unit cell that could supply more than 100 mA per NanoPad, with a theoretical 1.6 A maximum per Unit-Cell (16 FLR according to Figure 3.3), with adequate integrated power distribution. That amount of power fed by the linear regulator over a 560 µm×560 µm Unit-Cell, implies considerable heat dissipation through the wafer. This is due to the fact that the maximum power efficiency of a linear regulator is $(V_{OUT})^2/(V_{DD})^2$. This fact limits the one rail approach in terms of the maximum output power that every NanoPad can provide within a small silicon area (such as a Unit-Cell).

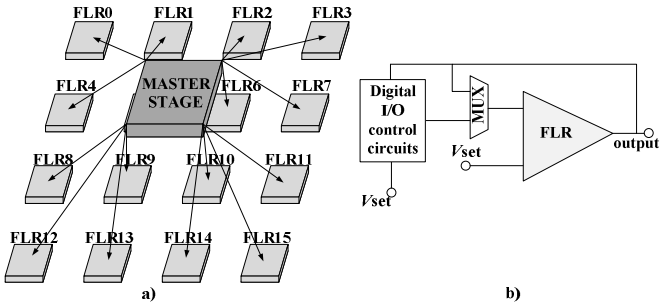


Figure 3.3 (a) The master-slave topology proposed in [3] where a master stage feeds to 16 fast load regulators (FLR) a common reference voltage. (b) The embedded digital I/O proposed in [3] where the feedback signal is either controlled by the FLR or the digital I/O control circuits.

3.3.2.3 A Multi-Rail Power Supply for Power Efficiency Improvement

To maximize efficiency of the embedded FLR a multi-power supply rail was proposed in [8], where a multilevel converter using a single power supply rail is used to generate several output voltage levels using a multiplexed voltage supply or stacked voltage cells (independent cells put in series where the output voltage is a combination of them). This multi-rail approach can increase the power efficiency by 49 %. This efficiency depends on the source power supply and

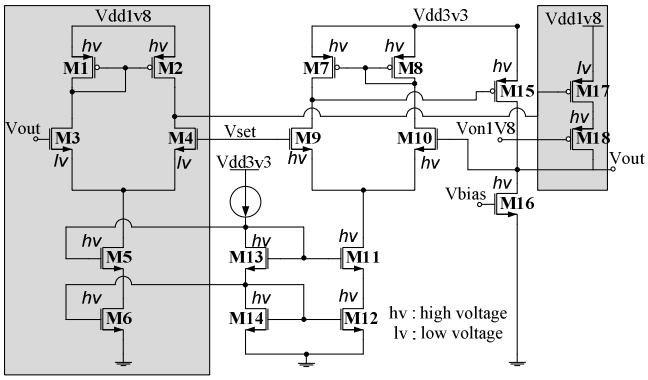


Figure 3.4 Previous version of a dual rail regulator with separate feedback loops [10].

output voltage, with a maximum of 50 W of instantaneous power. Unfortunately this approach uses discrete components that make it incompatible with our embedded FLRs, where a fully integrated solution is required.

One of the drawbacks of such multiplexed approach is that it requires different power supply rails. The WaferIC is supplied from the bottom of the wafer using TSVs [3]. Studies in [9] show that the number of TSVs must be selected based on a trade-off between IR drops within the power grid and the mechanical aspects of the wafer itself. Having more vias makes the wafer more fragile. It was found that TSVs density must be limited to 0.25 TSV/mm^2 with our technology [9], which makes the addition of more power rails (as suggested in [8]) impossible.

A second drawback of the solution proposed in [12] is the maximum power it can supply in a sustained way. Each NanoPad has to push several milliamps (50 mA) to meet the WaferIC requirements listed in Tableau 3.1. The proposed stacked voltage approach requires charge-pumps, which would introduce a lot of noise in the supplied power and ultimately limit the maximum current capabilities that can be obtained from the available silicon area.

3.3.2.4 A Configurable Power I/O PAD with Multi Power Rail Fast Load Regulator

To overcome the constraints on power distribution, silicon area, quiescent current and minimum required efficiency, a multi-power rail FLR is proposed. A preliminary version was proposed in [10] (Figure 3.4) where a FLR uses dual 1.8 and 3.3 V rails with an overall improvement of 40% of the power efficiency when operating at low voltage (1.0 V) compared to the solution with only

a single 3.3 V rail [10]. A drawback of this multi-power rail FLR is the duplication of all control circuitries used to assert the FLR, which is costly in terms of silicon area. Another drawback is that this architecture is optimized to operate at low voltages (such as 1.0 V) where 80 % of the current is provided by the 1.8 V rail [10]. This contribution from the lowest voltage rail to the output current drastically decreases as the output voltage gets close to 1.5 V, where the 3.3 V rail supplies most of the power. Notice that no mechanism is provided in this circuit to limit the current from the power supplies. A complementary solution is proposed in this presented paper where a single rail can be selected to minimize heat dissipation and silicon area.

With the solution proposed in Figure 3.5 and Figure 3.6, a silicon area similar to that reserved for the power transistors in the solution proposed in [3] will be used, where power rails are scaled down to handle only half the maximum current capability of the solution in [3]. This architecture benefits from a configurable control loop, power supply and bulk biasing. The principle is that when lower output voltages are required at the NanoPad, the 1.8 V rail is activated for a maximum theoretical efficiency from 55 % up to 83 % (1.0 and 1.5 V output voltages).

A challenge with multi power rail systems is the potential for latch-up. To prevent any possibilities of latch-up, protection transistors (switches) were added. With these transistors, it is possible to ensure that only one power rail at a time is tapped. Specifically, transistor M14 (Figure 3.6) must be turned off when V_{OUT} (drain of M14) is larger than the branch power supply V_{DDn}. M14 is turned off using the voltage V_{BASE} that provides static bulk biasing for M13 and M14 and that also feed the control loop with the suitable supply voltage. When the V_{DDn} rail is in operation, M13-M14 bulks (V_{BASE}) are set to V_{DDn}. When not in operation the bulks are biased at the highest voltage, V_{DD1}. Tableau 3.2 summarizes key characteristics of a previously reported solution and of the proposed solution for a configurable power I/O pad suitable for the WaferIC described in this section. It shows that for the same silicon area the proposed solution offers an

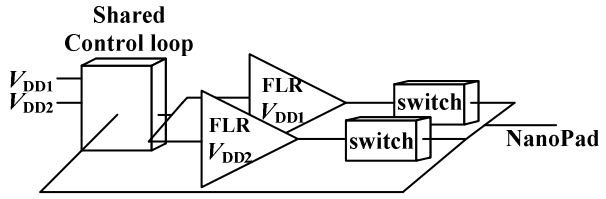


Figure 3.5 Multi-power rail FLR sharing a common configurable control loop

extended output range, better power efficiency, and comparable I/O speed but at the cost of a smaller maximum output current per rail (50 mA instead 110 mA). However, the same power is still available throughout the whole WaferIC.

3.3.3 Multi-Power-Rail Regulator Architecture and Circuit Implementation

This section details the circuit implementation for the proposed the multi-power-rail voltage regulator and I/O. It corresponds to a fabricated dual power rail, which can be extended to a multi-power rail configuration. The proposed architecture combines two separate fast load regulators operating with two power supplies (1.8 and 3.3 V). It is possible to operate one FLR at a time while sharing the same voltage feedback loop. Switches and dynamic bulk biasing are also added to prevent latch-up and ensure a good isolation of the non-operating FLR. The total current budget can be divided by the number of implemented power rails. In our particular case, a 110 mA total possible current is divided over 2 power rails occupying the same silicon area. This multi-power-rail regulator uses one common voltage reference generated in each Unit-Cell by a configurable bandgap in the master stage (Figure 3.3) as in [3]. This bandgap based voltage reference nominally produce the same voltage throughout the entire silicon wafer, in order to produce a steady operating voltage on V_{OUT} when the temperature increases or when there are slow variations (<kHz) in the power supplies.

Tableau 3.2 Comparison of previously reported and proposed solution of power I/O pad for a single or multi-power-rail.

	Previous Solution [3]	New solution
Active Silicon Area	110 µm×77 µm	110 µm×77 µm
Power Supply	3.3 V	1.8 and 3.3 V
Maximum output current	110 mA	50 mA (each rail)
Power efficiency @ 1.0 V	~30 %	~55 %
Power efficiency @ 1.5 V	~45 %	~83 %
Possible regulated output	1.0 to 2.5 V	0.5 to 2.995 V

voltages		

3.3.3.1 Multi-Rail Voltage Regulator Circuits

The proposed multi-rail voltage regulator combines several separated feedback loops into one (two in the presented paper). According to the desired output voltage, determined by V_{SET}, (0), the regulator can be configured to use either one of the two implemented supply rails, which are designed to operate at 1.8 V and 3.3 V, in order to limit the energy dissipated into the WaferIC. A main objective of combining both loops is to share circuits as much as possible. As listed in Tableau 3.1, the useable active silicon area of a NanoPad is 0.00847 mm^2 for a 0.18 µm CMOS technology implementation. Sharing the large transistors found in the control loop, such as M1 to M4 and M7 to M10 (Figure 3.4) results in savings of a 45×20 µm^2 per rail, which represents 11 % of the total available silicon area for a NanoPad. With the proposed circuit implementation, adding a power rail marginally increases the silicon area since few small size transistors (such as M5 to M7) are added, as well as another one for V_{BASE} selection.

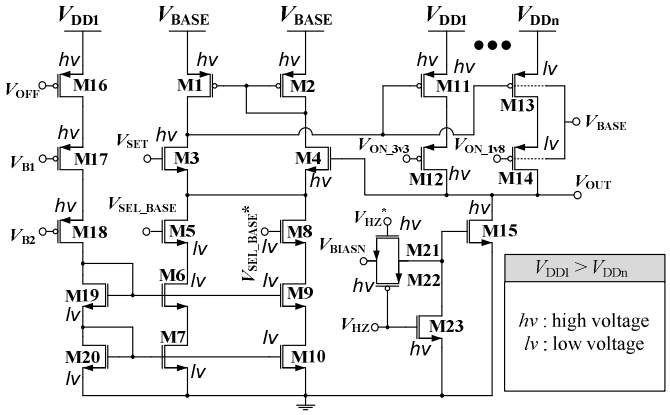


Figure 3.6 Transistor level of the proposed configurable multi-power rails FLR with 1.8 and 3.3 V power rails.

The whole configurable feedback loop shown in Figure 3.6 is made of transistors M1 to M10, where M1 and M2 form a simple current mirror, while M3 and M4 form a differential pair comparing V_{OUT} (the regulated output voltage shown in Figure 3.6) and input V_{SET}. The output voltage V_{OUT} is fed back through M4 and the transistors in the branches V_{BASE} and GND are powered by V_{BASE}. The voltage V_{BASE} is connected to either 1.8 V or 3.3 V, according to the

desired tapped power rail, using the digital signal V_{SEL_BASE} (Figure 3.7). The biasing of the control loop is asserted by two independent and mutually exclusive branches formed by M5 to M7 when $V_{BASE} = 3.3$ V, and by M8 to M10 when $V_{BASE} = 1.8$ V (Figure 3.6). The branch selection is controlled by the digital signals V_{SEL_BASE} and V_{SEL_BASE*}, its complement connected to M5 and M8 respectively. This design adequately biases the relevant differential pair according to the power rail connected to V_{BASE} to optimize the transient response and slew-rate of V_{OUT}.

A proper bulk biasing also has to be set according to the selected power rail to avoid latch-up. When V_{BASE} is connected to the 3.3 V rail, the bulk of M14 (low-voltage transistor) is set to $V_{BASE} = 3.3$ V. Indeed, if V_{BASE} was connected at 1.8 V direct biasing of the drain to substrate junction would occur and current would be fed to the substrate when V_{OUT} is larger than 1.8 V. Transistor M15 is biased with V_{BIASN} so that it always sinks a small current (hundreds of micro-amps) to activate the control loop and set V_{OUT} to the desired V_{SET}.

3.3.3.2 Quiescent Current Management

Reducing quiescent current of inactive modules to leakage levels is essential in the WaferIC. For example, in our application, a low quiescent current of 100 µA per NanoPad times 1.2 million of them in a 200 mm wafer would give a total static consumption over 100 A. A tenfold decrease in this quiescent current is possible but it would significantly degrade the slew-rate and transient response of the control loop and the FLR performance would degrade accordingly. Desirable as it is from a static consumption standpoint it is highly undesirable from a dynamic performance standpoint. A new approach is proposed here to allow a relatively high quiescent current in active NanoPads, while keeping the overall total current low.

To minimize static power dissipation, only NanoPads in contact with uIC's power pins are

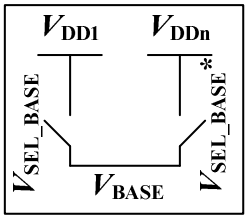


Figure 3.7 Configurable power supply for the control loop and transistor biasing. Switches are made of large pMOS

activated. These active NanoPads represent a small fraction of the NanoPads. A shut-down or sleep-mode approach is more amenable to bring the quiescent current of inactive NanoPads close to 0 A and therefore to control the overall static power consumption. When a NanoPad is in its OFF mode, the sinking current is in the magnitude of nanoamps, leaving a greater amount of available power for the active NanoPads (milliamps). For example, a Virtex 5 FPGA with a FF323 BGA package has 36 power pins, or 12 % of its relevant uIC pins [11]. When converting this into a NanoPad occupancy rate over the prototyping platform, this number decreases dramatically. For instance, a 40×40 mm^2 package covers an array of 71×71 Unit-Cells that comprise 80 656 NanoPads. If every pin of the package is in contact with 4 NanoPads it would result in an overall 1.6 % array occupancy for the 323 pins or 0.18 % for the power pins. Taking this into account, a turned ON FLR in the NanoPad could benefit from sufficient current headroom (milliamps) to perform its task. Thus, only a small fraction of the NanoPads would be drawing some biasing current, which allow improving the FLR performance by using larger quiescent current when needed.

The FLR sleep mode is activated first by cutting off the biasing branch of the control loop with the digital signal V_{OFF} and transistor M16 in Figure 3.6. The remaining of the circuit power consumption is disabled by turning off both the output current path with V_{ON_1v8} and V_{ON_3v3} signals using M12 and M14 respectively. Another digital signal, V_{HZ}, has been added to prevent any current path to the ground through M15. Activating V_{HZ} puts the M15 transistor in its cut-off region by shorting its gate to GND with M23 and deactivating the transmission gate formed by M21 and M22, placing the whole multi-power rail FLR in a high impedance mode and thus drawing virtually only transistor leakage currents (nanoamps).

3.3.3.3 Configurable Digital Input/Output NanoPad

As stated in the introduction, when a NanoPad is configured as an I/O rather than a power supply, to support CMOS I/O signaling, it has to accommodate wide range of standard I/O voltages from 0.9 V to 3.3 V according to the uIC balls in contact with it. The use of I/O banks such as the ones found in FPGAs [11] is not a suitable solution for the WaferIC. It would require at least one voltage reference per Unit-Cell adding, an extra 77 824 TSVs. Another approach has to be used to fulfill the voltage configurability of the I/O. Most configurable I/O, like the ones in FPGAs, offer a wide range of I/O output drive such as 2, 4, 6, 8, 12, 16 and 24 mA [11] to accommodate

different loads, fanouts, or PCB lines length. However, since a uIC ball is always directly connected to a NanoPad (direct connection), only the current sank by the load should be considered.

As mentioned in section III a, this paper proposes a small size multi-power rail FLR, combined with a multi-power rail I/O embedded in a configurable NanoPad interface circuitry. The reported implementation has two power rails (see Figure 3.8). Previous work in [3] proposed a combined version where the digital I/O uses the main FLR as its configurable power source. However this method requires additional control transistors and adds a significant parasitic capacitance load on the gate of the pass transistor (transistor that supplies power), making the response time of the FLR slower. By separating these two functionalities, the response time of the main FLR does not suffer from this added capacitance.

The proposed I/O circuit has its output (v_{OUT}) connected with the 40 mA-FLR (the one with high current capabilities in Figure 3.6) used for load regulation. The output voltage produced by the FLR ranges from 0.5 to 3.3 V, defined or set with the configurable signal V_{SET}, which is generated by a configurable bandgap reference (not discussed in this paper). The I/O was designed to offer a maximum current drive of 4 mA to fit the silicon area constraints. As shown in Figure 3.8, the power fed by the 4 mA-FLR (V_{DD_IO}) supplies the I/O made of transistors M24 and M26 for the high voltage rail (3.3 V) and transistors M25 and M27 for the low voltage rail (1.8 V). Buffers drive the gates of each transistor with control signals $V_{ON\_IO\_3V3}$ and $V_{ON\_IO\_1V8}$ to ensure that only one path is active at a time. The output can also be placed in a high impedance state with the control signal *OE*. The signal v_{IN_WN} is a digital data signal coming from the

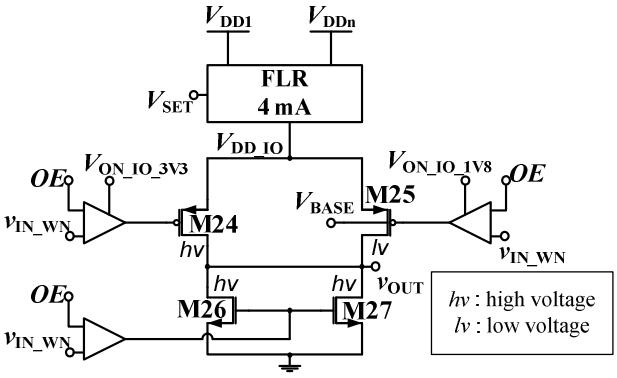


Figure 3.8 Proposed configurable dual rail digital I/O 4 mA output drive.

WaferNet and propagating to the NanoPad output v_{OUT}. These buffers allow the low drive capability of the signal v_{IN_WN} to drive larger transistors such as M24 to M27. The identical high voltage transistor M26 and M27 have two functions : save silicon area and extend lifetime of M27. Effectively, having a single ground (digital level '0') for all configurable V_{DD_IO} allows a reduction of the needed silicon area at the cost of I/O speed when operating at lower voltage such as 1.0 V. However, using low-voltage transistor at M27 would have degraded its lifetime when v_{OUT} >1.8 V. The NanoPad digital input operation is done by a digital CMOS buffer (not shown). This buffer receives any digital input signal with V_{HIGH} between 0.9 V and 3.3 V, and it scales up or down the input voltage to a clean 1.8 V digital CMOS signal.

3.3.4 Implementation and Experimental Results

To validate the proposed solution a test chip was designed and fabricated using TSMC 0.18 µm 6 metal layers CMOS technology. A microphotograph shows the actual fabricated chip (Figure 3.9). The circuits includes a complete configurable dual rail FLR with power supplies of 1.8 and 3.3 V, a configurable dual rail digital I/O, and a configurable bandgap that can produce and output value ranging from 0.9 up to 2.8 V for setting V_{SET} and others test circuits. The active area occupied by the FLR and the I/O is 100×80 µm for a total area of 0.0080 mm^2. The following section presents the experimental results regarding the main FLR, the maximum DC current for both rails for a wide range of output voltages, the regulation characteristics with an active load and the power supply noise rejection. Experimental results are also detailed for the embedded dual rails digital I/O.

3.3.4.1 DC Characterization

In the implemented design, the two power rails were not identically sized to provide the same amount of current. Indeed in most designs, uIC I/Os are powered-up at voltages higher than the uIC cores and more current is required by uICs cores (operating at the lowest voltages), thus the 1.8 V power rail was designed to have a current rating larger than the 3.3 V power rail. Figure 3.10 and Figure 3.11 show the DC characterization of the FLR for the 1.8 V and 3.3 V rails respectively. When the FLR is configured to use the 1.8 V rail, it can provide up to 60 mA with an output voltage as low as 500 mV using a single power supply. The average DC resistance for both rails is close to 4 Ω. The WaferIC structure forces a uIC pin to be in contact with a

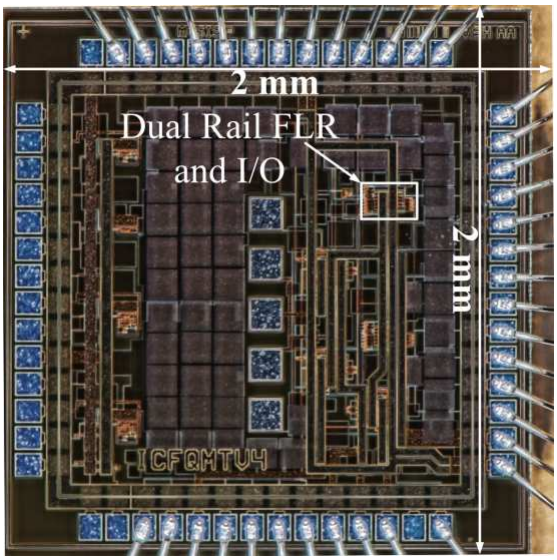


Figure 3.9 Microphotograph of the fabricated testchip of the proposed multi-power rail power pad and I/O in a 0.18 µm technology.

minimum of 2 NanoPads. A Virtex 5 FPGA with a FF323 BGA package has uIC balls of 500 µm of diameter [11]. In this case a single supplied ball would most certainly be in contact with around 10 NanoPads according to their geometries and sizes, which drops the overall DC resistance to 400 mΩ by having 10 FLRs working in parallel.

3.3.4.2 Response to an Active Current Load

According to the author in [12], the core capacitance of the power grid of a digital circuit in a 0.13 µm CMOS technology with a silicon area of 35 mm^2 has a typical value ranging from 14 to 30 nF. Smaller circuits can show smaller core capacitance down to ~2 nF. Our measurements were done with an equivalent core capacitance load of 4.7 nF, depicting an average size digital circuit, in parallel with an active current load that switches from 0 to 40 mA every cycle, with a 50 % duty-cycle. Transient characterization was performed at 3 different operating frequencies : 150 Hz, 1 MHz and 15 MHz for both power rails. A current output load of 40 mA with a 4.7 nF capacitance was used for all experiments, except when V_{OUT} is set to 2.60 V where the capability of the 3.3 V rail is not sufficient (according to Figure 3.11). In this case, a 0 to 25 mA load was applied.

Figure 3.12 (a) and (b) show a measured regulated $V_{OUT} = 0.85$ V and 2.0 V when the FLR is powered by the 1.8 V and the 3.3 V rails respectively. Tableau 3.3 summarizes the performance

results. We observe that both power rails offer similar performance regarding the output voltage deviation (ΔV_{OUT}) and dynamic output impedance ($\Delta V_{OUT}/\Delta i_{OUT}$). They respectively range from 120 mV up to 200 mV and 3.0 Ω up to 6.6 Ω. The WaferIC would most certainly have several NanoPads in contact with a load (uIC ball), which would reduce the dynamic output impedance according to the number of FLRs working in parallel, boosting in proportion the performance reported in Tableau 3.3.

Tableau 3.3 Performance summary of both power rail FLR with a dynamic load.

1.8 V power rail						
V_{OUT} (V)	0.850		0.900		1.50	
Current (ma)	40		40		40	
ΔV_{OUT} (mV)	150Hz	120	150Hz	160	150Hz	160
	1MHz	160	1MHz	160	1MHz	160
	15MHz	160	15MHz	160	15MHz	160
Dynamic output impedance (Ω)	3.0 to 4.0		4.0		4.0	
3.3 V power rail						
V_{OUT} (V)	1.50		1.80		2.60	
Current (mA)	40		40		30	
ΔV_{OUT} (mV)	150Hz	180	150Hz	160	150Hz	160
	1MHz	200	1MHz	200	1MHz	200
	15MHz	180	15MHz	180	15MHz	180
Dynamic output impedance (Ω)	4.5 to 5.0		4.0 to 5.0		5.3 to 6.6	

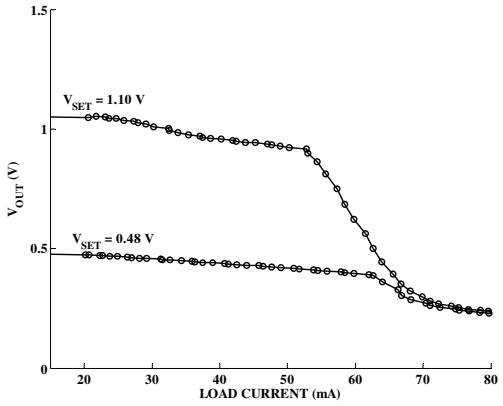


Figure 3.10 DC characterization of the 1.8 V power rail low-dropout regulator

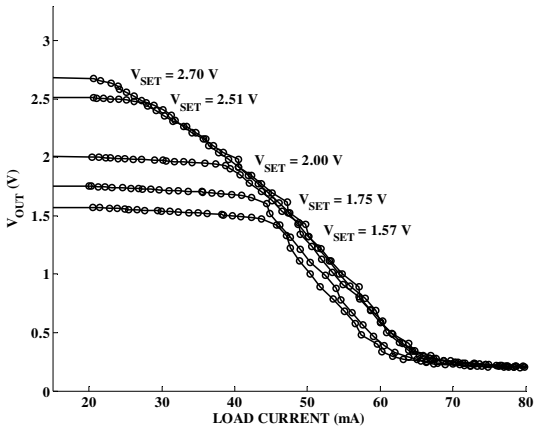
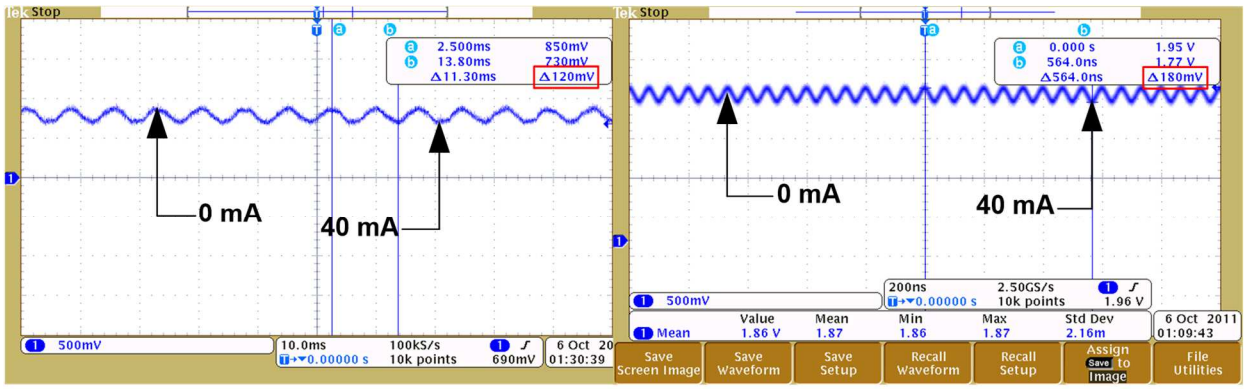


Figure 3.11 DC characterization of the 3.3 V power rail low-dropout regulator

3.3.4.3 Output Regulated Voltage Swing Capabilities and Quiescent Current

The proposed multi-power-rail regulator must be able to accommodate any uIC deposited on its active surface in terms of power distribution, meaning that the regulated voltages should support a wide range of V_{DD}. Figure 3.13 demonstrates the output capabilities of the proposed architecture in relation with the applied V_{SET}. The measurement clearly shows a linear relation between V_{SET}



a) b)

Figure 3.12 Transient v_{OUT} response (Figure 3.6) to a 0 to 40 mA current load with a 4.7 nF output capacitance (a) when supplied with the 1.8 V power rail for 150 Hz at V_{OUT} = 0.85 V. (b) when supplied with the 3.3 V power rail to a load of 40 for 15 MHz at V_{OUT} = 2.0V.

and V_{OUT} with a small DC offset less than 100 mV. The proposed system saturates at ~3.0 V in terms of regulated output voltage.

Each unused FLR can be turned off for minimum power consumption. By doing so, the leakage current drops to ~120 nA drawn on the 3.3 V power rail and as little as 25 nA on the 1.8 V rail. This low current consumption allows the proposed architecture to be integrated into a full wafer device. The overall maximum leakage current is 155 mA on the 3.3 V rail and only 31 mA on the 1.8 V rail.

3.3.4.4 Digital I/O Characterization

The proposed design implemented in the test chip also includes the embedded configurable digital I/O, described in Figure 3.8, which shares the output (v_{OUT}) with the FLR. A high impedance configuration mode is a necessity for both structures to ensure that the regulation and I/O do not interfere with each other. The high voltage level produced by the digital I/O can range from 0.5 up to 3.3 V. Measurements shown in Figure 3.14 were obtained when the configurable I/O is configured to produce output voltages of 0.5, 1.0 and 1.5 V using the 1.8 V power rail. We notice that the operating frequency depicted in Figure 3.14 is 250 kHz. This low frequency is related to the test bench. Since both regulation and digital I/O functionalities physically share the same output on the testchip, and the test environment was optimized for power delivery test, the maximum operating frequency is dramatically reduced due to all the extra parasitic capacitances introduced (~50 pF). Post-layout simulations including all parasitic capacitances and inductances were performed using Cadence and Calibre tools. It was found that the maximum operating frequency of the digital I/O is 250 MHz when the actual current drive of 4.2 mA is applied to a 5 pF load, which represents the typical capacitance of a uIC pin and bounding wire for a digital I/O [12].

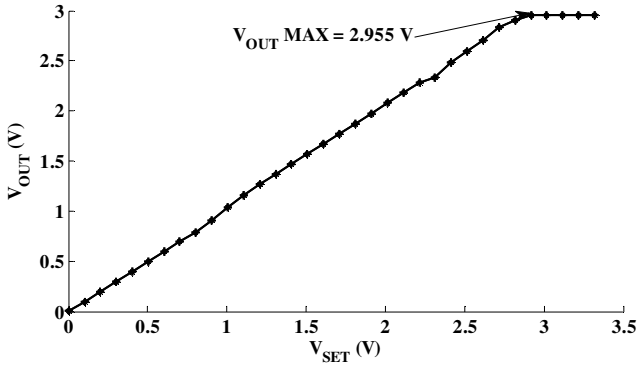


Figure 3.13 Relation between the output voltage (V_{OUT}) and the configured voltage V_{SET}, of the proposed multi-power rails voltage regulator.

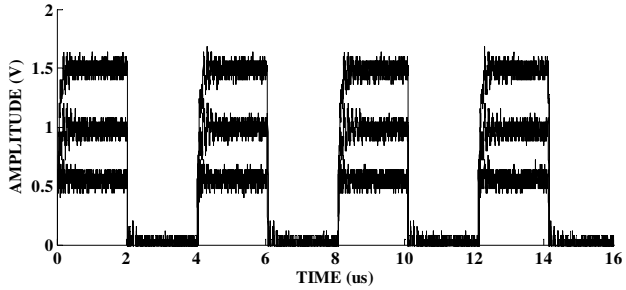
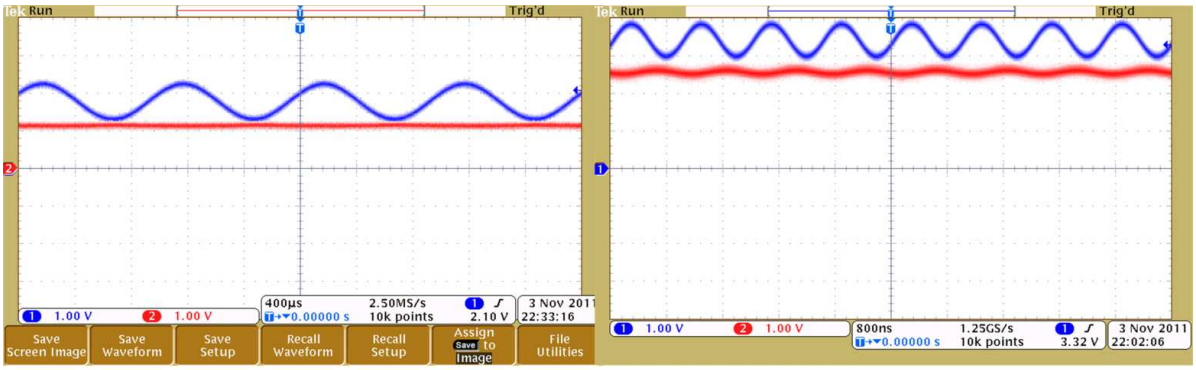


Figure 3.14 Measured output voltage of the configurable digital I/O configured to provide 0.5, 1.0 and 1.5 V CMOS output voltages for a 250 kHz input signal.

3.3.4.5 Power Supply Rejection Ratio

Both power rails need to be insensitive to fluctuations on their own respective power supplies. Measurements were performed on both rails by injecting a sinusoidal signal superposed to a DC voltage of 1.8 or 3.3 V and by observing the output v_{OUT}. Figure 3.15a shows V_{OUT} = 1.0 V with noise injection on the power supply corresponding to $V_{DD} = 1.8\ V_{DC} + 1\ V_{pp}$. At 1 kHz, we observe virtually no disturbance in the output voltage with more than -40 dB of noise rejection for this frequency on the 1.8 V power rail. The same measurements were performed at 10 kHz and 1 MHz with a slight change of stimulus ($V_{DD} = 1.8V_{DC} + 0.8V_{pp}$). The decrease of the sinusoidal input amplitude to 0.8 V in only due to equipment limitations at this frequency Again measurements show a noise rejection of more than -40 dB at 1 MHz. Tableau 3.4 list the power supply rejection ratio (PSRR) of both rails.



a) b)

Figure 3.15 Output voltage vOUT (red) when sinusoidal noise is injected on power rail (blue): (a) 1.8 V power rail with VOUT = 1.0 V at 1 kHz. (b) 3.3 V power rail with VOUT =2.5 V at 1 MHz.

Figure 3.15b depicts a similar scenario but with a $V_{OUT} = 2.5$ V using the 3.3 V rail where V_{DD} =3.3 V_{DC} + 1 V_{pp}. Measurement shows similar noise rejection at lower frequency (1 kHz) between both rail, around -40 dB of noise rejection. A slight increase of the output noise occurs at 10 kHz where the noise rejection reaches -30 dB and -25 dB at 1 MHz.

Tableau 3.4 Performance summary of both power rail PSRR

1.8 V power rail		
V_{OUT} (V)	0.9 and 1.0	
V_{DD} (V)	1.8 V_{DC} + (1.0V_{pp}/0.8 V_{pp})	
PSRR (dB)	1kHz	-40
	10kHz	-40
	1MHz	-42
3.3 V power rail		
V_{OUT} (V)	2.0 and 2.5	
V_{DD} (V)	3.3 V_{DC} + (1.0V_{pp}/0.8 V_{pp})	
	1kHz	-40

PSRR (dB)	10kHz	-30
	1MHz	-25

3.3.4.6 Comparison with Existing Works

The proposed multi-power rails voltage regulator does not require any on-chip decoupling capacitor. This design is meant to work only with the parasitics conveyed by a uIC ball and its power grid (~1 nH, ~4.7 nF). This multi rail regulator offers a unique and novel possibility to draw power either from the 1.8 V or 3.3 V line resulting in power saving up to 25 % compared to a single rail design (as proposed in [3]).

Equation (1) gives the response time T_R calculated from the load (C_{LOAD}) the maximum voltage deviation (ΔV_{OUT}) for the 1.8 V power rail at 0.9 V operating at 15 MHz and the maximum current the regulator can provide (I_{MAX}). The measured response time with our design parameters is 21.1 ns.

$$T_R = \frac{C_{LOAD} \cdot \Delta V_{OUT}}{I_{MAX}} = \frac{4.7\ \text{nF} \cdot 80\ \text{mV}}{40\ \text{mA}} = 21.1\,\text{ns} \qquad (1)$$

For comparison of various FLR, the Figure of Merit (*FOM*) described in (2) is used, where I_Q is the quiescent current [7]. As shown in Tableau 3.5, this work achieves the best *FOM* by a hundredfold as well as being the most compact architecture even with a digital I/O integrated within its structure.

$$\begin{aligned} FOM &= T_R \frac{I_Q}{I_{MAX}} \cdot APB \\ &\Rightarrow 21.1\,\text{ns} \cdot \frac{126\,\mu\text{A}}{40\ \text{mA}} \cdot 0.0002 = 0.0000133\ \text{ns} \end{aligned} \qquad (2)$$

This work also achieves the widest regulated output range with almost 2.5 V, compare to 0.8 V for its closest competitor [13]. Moreover, this proposed architecture allows power saving when operating at lower voltages by using the adequate rail to minimize heat dissipation and greater power efficiency compared to its previous version. Power saving up to 25 % is achieved for V_{OUT} = 1.0 V and 30 % for a V_{OUT} = 1.2 V, while being more efficient in terms of silicon usage.

Tableau 3.5 Performance comparison of the proposed FLR with different works

	[7]	[13]	[14]	**This Work**
Year	2005	2010	2012	2014
CMOS Process (µm)	0.09	0.18	0.065	0.18
Area (mm^2)	0.098	0.006	1.0908	0.0080
V_{IN} (V)	1.2	1.8	1.1	1.8 or 3.3
V_{OUT} (V)	0.9	0.9 to 1.7	0.5 to 1.0	0.5 to2.955
I_{MAX} (mA)	100	20	100	40
I_Q (µA)	6000	1.06	164.5	0.000145
Response Time T_R (µs)	0.00054	0.0015	0.0054	0.02115
Decoupling capacitor (µF)	0.00060	0.0005	0.0045	0.0047
FOM (ns)	0.0000314	0.0000632	0.0000969	0.0000133
Area per mA	0.00098	0.0003	0.010908	0.0002

3.3.5 Conclusion

A platform for rapidly prototyping electronic systems, the WaferBoard™, is being developed in our lab. It is based on a configurable wafer-scale active circuit. Electronic components firmly held in contact with its surface are powered and interconnected using circuits implemented in this active surface. This paper focuses on means for power delivery that mitigate heat dissipation by introducing a novel multi-power rail voltage regulator that operates from 1.8 V and 3.3 V rails. The addition of second power rail allows power savings up to 25 %, while offering a wider range of operation at the cost of reducing the total deliverable power per rail due to limitations in the available area. The proposed design merges two fast load regulators into one by using configurable power supplies, the bulk biasing technique and shared transistors. The proposed

architecture was fabricated in a 0.18 µm CMOS technology and occupies a small area of 0.0080 mm^2 by combining the two control loops into one, which makes it suitable for wafer-scale integration. Moreover, the proposed design offers a fast response time of 21.1 ns, with a 40 mA load on either supply rail, and very low quiescent currents of 126 µA. This work also achieves the best Figure Of Merit that outperforms by a factor of 3 its closest competitors.

CHAPITRE 4 CONCEPTION D'UN TAMPON ANALOGIQUE CONFIGURABLE

4.1 Résumé

Le WaferIC dans sa version initiale ne dispose que de plots numériques tel que mentionné dans le chapitre 1 et 2. Un premier ajout majeur au WaferIC est l'ajout à ce dernier de la possibilité de propager des signaux analogiques d'un NanoPad à un autre. Indépendamment de la technique utilisée pour transmettre ce signal, le NanoPad en mode réception doit pouvoir attaquer une charge constituée de la bille et toutes ses capacités, résistances et inductances parasites. Pour ce faire, l'ajout d'un tampon analogique « *analog buffer* » à la sortie d'un NanoPad est nécessaire.

Toujours en conservant l'optique que le WaferIC est un circuit « *wafer-scale* », la surface de silicium occupée demeure la contrainte la plus aiguë lors de l'ajout d'un circuit. D'autres points nécessitent également une attention particulière. La taille du réseau de distribution de puissance du WaferIC est considérable, signifiant que la tension sur la surface d'un Réticule varie d'un point à l'autre dus aux résistances parasites des lignes de métal intégrées le constituant. Ces parasites rendent donc les grilles d'alimentation susceptibles à l'injection de bruit et aux chutes de tension DC.

L'article « *A Configurable Analog Buffer Dedicated to a Wafer-Scale Prototyping Platform* » est un article sur invitation publié en Janvier 2015 pour la revue « *Springer Science & Business Media Analog Integrated Circuits and Signal Processing* » des suites d'un article présenté à la conférence « *Latin American Symposium on Circuits and Systems* » LASCAS 2013. Cet article propose une nouvelle architecture d'un tampon analogique utilisant deux étages complémentaires nMOS et pMOS ce qui permet d'améliorer la plage dynamique de la tension de sortie. Chaque étage est constitué d'une paire différentielle modifiée et lorsque combinée démontre un gain quasi unitaire. Le tampon proposé bénéficie également de la possibilité d'être configuré quant à sa tension de polarisation afin d'adapter ses performances à la bille et la charge qu'il doit piloter. La possibilité de varier sa tension de polarisation permet de n'utiliser que le courant nécessaire pour le bon fonctionnement de la transmission du signal analogique. Si une plus grande bande passante est nécessaire, le tampon s'adapte pour attaquer la charge avec une vitesse maximale de 194 MHz et un « *slew-rate* » de 495 V/µs avec un temps de réponse de 5.3 ns. Dans le cas de

contraintes de performances plus relâchées, cette vitesse peut être diminuée jusqu'à 74 MHz pour un « *slew-rate* » de 66 V/µs. L'ensemble du tampon implémenté en technologie CMOS 0.18 µm n'utilise que 21 transistors pour une taille totale de 0.001824 mm^2.

4.2 Contribution au domaine scientifique

La contribution majeure de cet article est la proposition d'une architecture nouvelle pour un tampon analogique possédant une bande passante appréciable, le tout dans une surface de silicium compacte. Ce tampon a également été un point tournant pour la conception de la référence de tension configurable, utilisée également comme CNA dans le prochain chapitre, puisqu'il réutilise une partie de l'architecture du tampon analogique.

4.3 Article #2 : A Configurable Analog Buffer Dedicated to a Wafer-Scale Prototyping Platform

***Abstract*—**This paper concerns a novel configurable analog buffer dedicated to a wafer-scale prototyping platform of electronic systems. The proposed architecture uses complementary nMOS and pMOS stage buffers, which are built with modified conventional differential pairs used for maximizing the output voltage swing. This compact analog buffer offers several slew-rate features that range from 66 V/µs up to 495 V/µs with a quasi-unity gain and only uses 21 transistors for a total silicon area of 0.001824 mm^2. The bandwidth of this proposed buffer can be programmed from 74 MHz up to 194 MHz with response time up to 5.3 ns. This overall configurability allows better power management, reduces the power-supply noise injection within the wafer-scale platform, and diminishes the quiescent current.

4.3.1 INTRODUCTION

THE WaferBoard™ is a recently introduced wafer-scale prototyping platform of electronic systems [1]-[3]. This platform acts as a configurable support for user integrated circuits (uICs), where any type of signal or power can be fed to the uICs balls in contact with. This wafer-scale platform is populated with a sea of small conductive pads called NanoPads, which can be configured independently as a ground, a regulated voltage output, a digital input-output (I/O) or as an analog I/O. NanoPads are grouped in 4×4 arrays called Unit-Cells, and arrays of 32×32

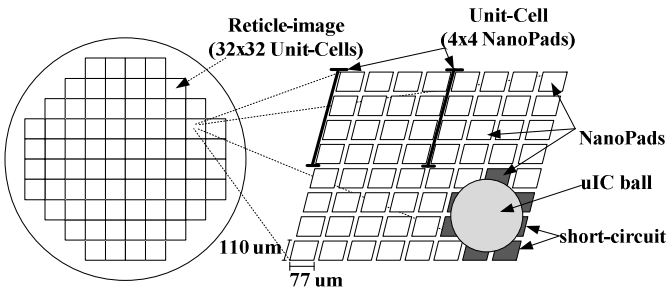


Figure 4.1 Hierarchical view of the WaferIC™, the reticle-image the Unit-Cell and the NanoPad.

Unit-Cells are called reticle-images (Figure 4.1). Inter-reticle stitching build an assembly of 76 photo-repeated reticle-images into a 200 mm wafer-scale platform named WaferIC. The specifications of this chosen architecture were defined by previous work in order to obtain a maximum coverage of the wafer surface with NanoPads while leaving enough silicon room for the needed circuits. This prototyping platform was thus designed to support any uIC package with 250 µm ball diameter and 800 µm pitch [1].

Each NanoPad is a fully configurable power pad and I/O, which can deliver up to 110 mA with various outputs voltage (0.9, 1.0, 1.2, 1.5, 1.8, 2.0, 2.5 and 3.3 V). When configured as an I/O, digital signals can propagate from a pad to any others within the WaferIC at a maximum frequency of 300 MHz and with the same output voltage as the power configuration defined previously (from 0.9 to 3.3 V) [3]. Signals communication between NanoPads is ensured by a dense fault tolerant network called WaferNet [4]. This network can send and receive signals in 4 directions (N, S, E, W) to/from neighbouring Unit-Cells using link of various lengths (1, 2, 4, 8, 16 and 32); where, for instance, a link of length 8 has 7 Unit-Cells between the two communicating Unit-Cells [4].

To propagate an analog signal between NanoPads within the WaferIC an analog to digital converter (ADC) and digital to analog converter (DAC) are needed. In this case a NanoPad samples the input analog signal and propagates it through the WaferNet as a digital signal. The receiving NanoPad converts back the original signal and outputs it. The conversion back to the analog world requires a buffer that can drive the load connected to it (the uIC ball) [5] [6]. Analog output buffers are commonly designed to drive a large capacitive load, to minimize the static power consumption (quiescent current) and often rely on the use of operational amplifiers

[7]. Other requirements such as the output voltage swing, rail-to-rail operation and the speed of the buffer are important criteria. Class-AB output buffer offers a good trade-off when low signal distortion, low quiescent current and good driving capabilities are the objectives. Other approaches found in the literature use push-pull [8], class-A [9] or class-B output buffer [10]. These approaches are limited in the overall speed because they imply a high impedance output node with drain connected transistors only to drive the output [11]. Hence a dedicated fast operation buffer requires a low-output impedance having a source connected topology with a drain and gate connected together is more amenable [11].

Each NanoPad embeds functionalities such as power supply and digital I/O, leaving very little silicon area available for an analog buffer. Despite the good performances that approaches published in [5]- [10], and [12] offer, to the best knowledge of the authors, none of them fits the space requirements of a NanoPad and the output capabilities that would suit the uIC ball in contact with it. A typical load consists of parasitic capacitances added by the uIC package, the printed circuit board (PCB) metal line and the internal capacitance of the integrated circuit itself. The WaferIC reduces this load because uIC ball lies directly over the NanoPad with no PCB lines which typically introduces an overall load by ~8 pF [12]. It is assumed that total capacitive load that the analog buffer, within the WaferIC, needs to drive is ~12 pF.

In this paper, we describe a compact low-power fast operating analog buffer with configurable slew-rates. As found in an FPGA digital I/O, this novel analog buffer has the capability to adjust its performance according to the load requirements (uIC). The main advantage is power-supply noise injection and total power consumption can therefore be minimized. Section II presents the power supply architecture of the WaferIC and the advantages for a configurable analog buffer. We present in section III the proposed analog buffer and describe the configuration capability. Sections IV and V describe post-layout simulation results and compare our circuit performance with other published works.

II-WaferIC Overview

The WaferIC is a made of a full configurable active 200 mm wafer in a 0.18 µm CMOS technology, which is capable of interconnecting the user integrated circuits deposited on its alignment insensitive surface. To do so the WaferIC can be configured to provide digital/analog links, or act as a regulated power-supply. The following subsections give an overview of the

WaferIC topology and its power distribution structure along with the challenges associated with it.

4.3.2 The WaferIC architecture

Figure 4.1 shows a hierarchical view of the WaferIC where NanoPads are the smallest configurable elements occupying an active area of 77 µm×110 µm. Grouped in Unit-Cell arrays, the NanoPads populate the entire 200 mm Wafer. Each NanoPad is a contact point that can be configured accordingly with the uIC ball that connects it. The WaferIC surface is also covered with an anisotropic conductive film (Z-axis film), which is based on embedded conductive vertical fibers (nickel needles) [4], to protect the fragile surface of the wafer and to ensure a good electrical and mechanical contact between the NanoPad and the uIC ball.

In order to locate a uIC ball deposited on the WaferIC surface a contact detection mechanism was implemented, by applying a weak pull-up at a NanoPad output and a strong pull-down to its neighbours (Figure 4.2). When a uIC ball creates a short-circuit between several NanoPads (minimum 2), the weak pull-up charge would be absorbed and this change can be detected using a XOR gate (detected short-circuits are shown on Figure 4.2). The uIC ball position can be deduced by scanning the whole WaferIC surface with a specific sequence and pattern of pull-up and pull-down and then mapping all the detected short-circuits (as in Figure 4.2).

4.3.2.1 The WaferIC power distribution network

The WaferIC is powered by two supply rails of 1.8 and 3.3 V, which are the typical supply

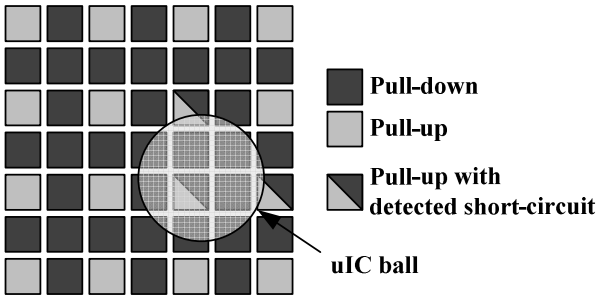


Figure 4.2 Contact detection mechanism using weak pull-up and strong pull-down, where detected short-circuits are shown where weak pull-up are absorbed by strong pull-down and causing a detectable anomaly.

voltages for 0.18 µm CMOS technology, through an integrated power grid distributed uniformly over the 200 mm wafer. The WaferIC power supply is based on an arborescent topology where a single printed circuit board (PCB) is the root and the NanoPads the leaves.

The main power, which comes from the main AC supply into a 12V DC power supply, travels through specially designed circuit boards called Power-blocks where it is down converted to standard supply voltages of 1.8 and 3.3 V and fed to reticle-images using through silicon vias (TSVs). A Power-block can supply up to 4 reticle-images with maximum current of 5 A and 20 A on 1.8 and 3.3 V rails respectively. The bottom-up power flow is shown on Figure 4.3.

The integrated grids shown in Figure 4.3 are linked through a full reticule-image while the grounds lines are common to the whole WaferIC. Any short on power rail due to defects implies that a full reticle-image circuit have to be disabled. In order to make sure that all circuits are working properly, sufficient voltage headroom must be considered from the root to the NanoPads supplies. Every stage has a DC voltage drop due to parasitic resistances. In our first order model, the main PCB is considered as a perfect electrical conductor because of the metal line thickness and decoupling capacitors. On the other hand, the TSV resistance was measured in [14] to be on average 11 mΩ. The integrated metal grid was chosen to fill the maximum available metal space on the wafer while respecting the design rule check (DRC) of the chosen CMOS technology (0.18 µm). To achieve that, the metal grid dimensions were chosen to be 6 µm in width with pitch of 30 µm [3] [14]. Several combinations of TSV density with the integrated metal density were simulated using COMSOL Multiphysics. A maximum overall acceptable DC drop at the NanoPads grid is 150 mV and the maximum density of TSVs is 1/mm^2. The upper limit of TSVs density is due to a mechanical limitation, where the more holes in the wafer the more fragile it is.

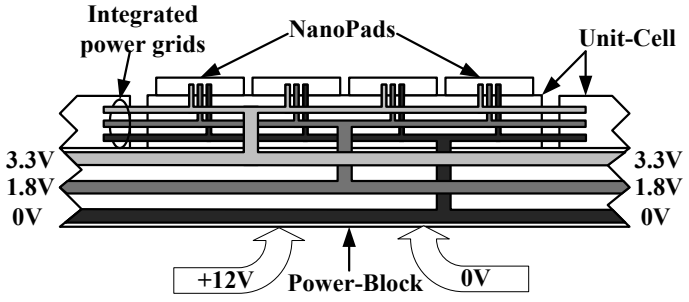


Figure 4.3 Power supply distribution of the WaferIC as an arborescence topology.

The chosen scenario is an integrated metal grid of 6 µm/30 µm (width/pitch) and a 0.25/mm^2 TSV, which gives an overall maximum voltage drop of 90 mV for an equivalent resistance of 257 mΩ [3].

The arborescent power structure combined with the size of the power rails and the number of circuits connected to it makes the power-supply voltages uneven across a reticle-image. This is mainly due to parasitic resistances, process variations or the large number of uIC balls that needs to be supplied and their random placement over the WaferIC surface. These physical and structural constraints could inject significant supply noise in the 1.8 V, 3.3 V and ground grids. The circuits chosen to be integrated within each NanoPad must take those issues into account in order to minimize the supply noise injection.

4.3.3 A Configurable Analog Buffer

Each NanoPad is an independent point of contact, which can ideally receive any type of uIC ball, and act as a regulated power supply, a digital I/O, or analog I/O. The available silicon area, of 77 µm×110 µm is then shared between all those needed functionalities. Existing solutions were already described in [3] for power delivery and the digital I/O footprint was occupying nearly 100 % of the available silicon area. The authors propose in this section a novel configurable analog buffer that fits the very aggressive silicon area requirements of the WaferIC and minimize the noise injection within the power supplies. The proposed solution for integrating an analog buffer has only 21 transistors and yields to a very compact structure of 0.001824 mm^2.

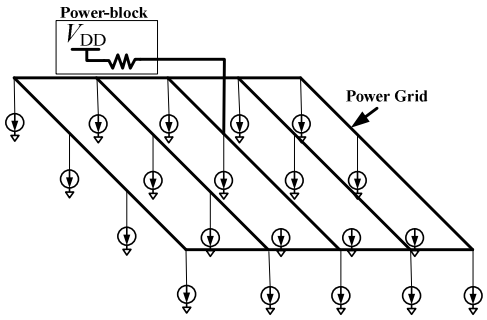


Figure 4.4 Simplified worst case model of the WaferIC power grid with an equivalent resistance of 250 mΩ in series with each active circuit (modeled as current source).

4.3.3.1 Power supply noise injection

The size of the WaferIC (200 mm) generates a typically large integrated power grid, which makes supplying all the circuits with a clean power-supply challenging. Any active circuit in any NanoPad or any uIC ball deposited on the WaferIC will induce noise into the power grid. This is due to the fact that the Power-blocks are not ideal voltage sources and that the LDO within can be seen as an ideal voltage source in series with a resistance.

The configurability of the proposed analog buffer is in respect of the main idea of power-supply noise injection diminution. As an explanation, a simplified worst case power-supply grid, which includes an equivalent serial resistance of, for example, 250 mΩ (a typical serial resistance for a discrete linear regulator) from the power supply to the loads, represented as current sources is shown in Figure 4.4. A 16 mA loads would create, a DC drop of 4 mV on the power grid. When scaling at the WaferIC level, the noise builds up with the number of operating active circuits. For example, one hundred 16 mA active circuits in parallel would sink 1.6 A with a DC voltage drop equals to 400 mV, which is 2.5 times more than the of 150 mV maximum drop stated in section II. This analysis shows that any active circuits (CMOS circuits connected to the power grid) will inject noise and that this noise needs to be minimized as possible in order to meet the maximum stated voltage drop of 150 mV on the V_{DD} rail.

4.3.3.2 Circuit of the proposed analog output buffer

The proposed analog buffer is made of two complementary and parallel buffer stages (Figure 4.5). Both stages work together to boost the output voltage swing. Transistors M1 and M2 from the nMOS stage are matched by M5 and M6 of the pMOS stage. The first buffer is completed by M3 and M4 and the second one by M7 and M8. Each analog buffer is based on a modified differential pairs where the output is tied by M4 and M6 gates, which are diode connected transistors (gate and drain shorted). This allows lowering the output impedance and boosts the buffer speed [11]. Transistor M1 and M2 are simple current mirror (the same for M7 and M8 in the pMOS stage), which ensures that both branches' current are equal allowing *vout* at the gate of M4 and M6 and the gate of M3 and M5 to match *vin*.

4.3.3.3 Small-signal analysis

The output voltage gain A_v of the proposed analog buffer (Figure 4.5) can be first estimated from the gain of the nMOS stage. Since both stages are in parallel, the overall gain can be expressed by either the nMOS stage or the pMOS stage when they are sized properly. The small signal analysis of the nMOS stage of the proposed analog buffer is shown in Figure 4.5 using the T model, where $id_3 = is_3$ and $id_2 = is_2$. Because both branch current are equal and that M3 matches M4, therefore we can say that $id_2 = -id_3$ and that $gm_3 = gm_4$. The current id_3 can be express by (1) where $g\mathrm{m}_n$ is the transconductance parameter.

$$is_3 = \frac{vin - vout}{1/gm3 + 1/gm_4} = \frac{gm_3(vin - vout)}{2} \qquad (1)$$

Output current i_{out} (current at *vout*) of the equivalent circuit shown in Figure 4.5 is given by $i_{out} = is_3 - is_2$ and yields to (2).

$$i_{out} = gm_3(vin - vout) \qquad (2)$$

Where *vout* can be expressed by $i_{out} \cdot r_{out}$ and where $r_{out} = rds_2 // rds_4$ and where rds_n is the drain resistance of transistor M_n, we can write :

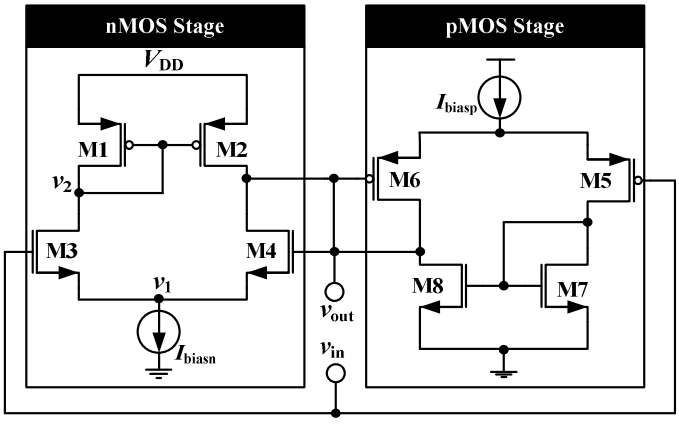


Figure 4.5 Proposed output buffer using nMOS and pMOS input transistors in two complementary parallel buffer stages.

$$v_{out} = gm_3 (vin - vout)(rds_2 // rds_4) \qquad (3)$$

Rearranging (3), the voltage gain (A_v = *vout*/*vin*) of the proposed nMOS stage is obtained and given by (3).

$$Av = \frac{gm_3 (rds_2 // rds_4)}{1 + gm_3 (rds_2 // rds_4)} \qquad (4)$$

A non-modified differential pair would result in a gain of $A_v = gm_3 \cdot rds_2 // rds_4$. Equation (4) yield a gain close to unity when $gm_3 = gm_4$ by scaling adequately those transistors. The same approach can be used for the gain of the pMOS stage. When both nMOS and pMOS stages can be made equally matched : i.e. both active stages are in parallel and benefit from each other advantages. In this case, the output voltage swing can be maximized. Equation (5) shows the dependency between the voltage gain Av and the biasing current I_{biasn}. When the slew-rate goes up, so is I_{biasn}, the system becomes faster at the expense of the voltage gain.

$$gm_n = \sqrt{\beta_n I_{D1}} = \sqrt{\beta_n \frac{I_{biasn}}{2}} \qquad (5)$$

4.3.3.4 Output voltage swing

The maximum output voltage swing is defined by both the nMOS and the pMOS stages shown in Figure 4.5. The nMOS stage stop operating in linear mode when transistors M2 and M4 go out of the saturation region, where $|V_{GS}-V_{THn}| = V_{DSATn}$ with V_{THn} being the threshold voltage of both nMOS transistors. The minimum voltage drop across M2 is the set to V_{DSATn}, meaning that the upper value of output voltage swing is $V_{DD}-V_{DSATn}$. On the other hand, the minimum operating voltage of M4 is $V_{DSATn}+V_{THn}$, meaning that the lowest operating voltage is $V_{DSATn}+V_{THn}$ (Figure 4.6). The pMOS stage is complementary to the nMOS stage, where the upper and lower limits of the output voltage swing are inverted. The upper limit value is set to $V_{DD}-V_{DSATp}-V_{THp}$ and the lower value to V_{DSATp} (Figure 4.6). Combining both nMOS and pMOS stages enhances the

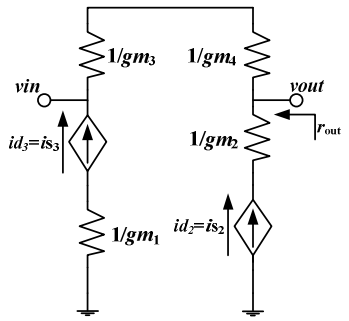


Figure 4.6 Simplified small-signal equivalent circuit of the proposed nMOS stage output buffer shown in Figure 4.5

maximum output voltage swing by an offset of V_{TH} toward V_{DD} and the ground. The output voltage swing is therefore limited between V_{DSATp} and V_{DD}-V_{DSATn}, with an average value of ~1.4 V for a 180 nm CMOS technology (V_{TH} = ~0.7 V) [16]. The value of V_{DSATx} depends mainly on the transistors sizes and the biasing current, the higher the current : the higher the current, the higher V_{DSATx} is.

4.3.3.5 Configurable slew-rate

Several types of different uIC balls might be in contact with the WaferIC surface with different analog characteristics such as speed, output voltage and load. One method to suit all demands would be to design a buffer with very high performance and current capabilities. However, as discussed in section III, the power supply noise injection is a factor that must be taken into account in wafer-scale integration where there could be several thousands of output buffers. An output buffer that can be configured in terms of slew-rate to match the uIC balls requirements is more desirable for the WaferIC, where the noise injection and power is an issue.

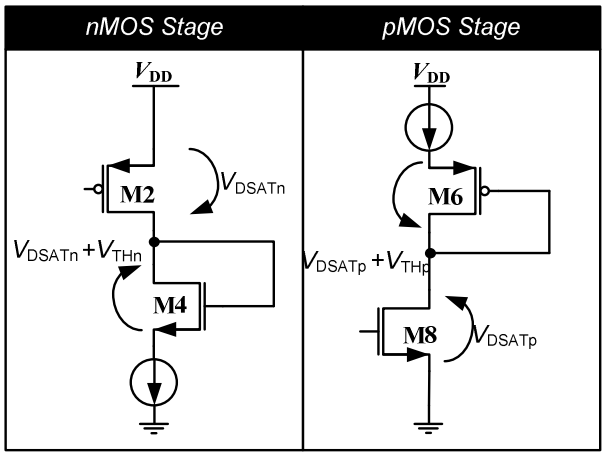


Figure 4.7 nMOS and pMOS voltage output swing higher and lower limits of the proposed complementary CMOS analog buffer.

The speed of an analog output buffer is defined by its slew-rate. Augmenting the slew-rate of an analog output buffer can be done by increasing its biasing current [17] at the cost of increased power-supply noise injection, higher quiescent current and the reduction of the maximum output voltage swing. This reduction is due to the fact that V_{DSAT} increases with the biasing current where the drain currents of M2 and M8 (Figure 4.5) are linked to the biasing current of the analog buffer as shown in (5). The slew-rate configurability is achieved by using an array of nMOS or pMOS (according to the stage) that can be connected or disconnect from the buffer. The current source of nMOS stage of Figure 4.5 can be expressed as an nMOS transistor (M9) with its gate biased at a fixed current I_{biasn}, as shown in Figure 4.8. This transistor can also be expressed as 3 different transistors with various sizes, M9-1 to M9-3, where M9-1 is always on for a fixed 2 mA I_{biasn} and two control bits (V_{on-2} and V_{on-3}) can enable two other biased transistors. For instance when V_{on-2} is high and V_{on-3} is low, V_{biasn} is connected to the gate of M9-2 (two times the size of M9-1) by transistor M10-2 for an additional 4 mA and M9-3 (two times the M9-2) gate is shorted to the ground by M11-1 disconnecting it from the overall circuits. To make slew-rate of the proposed analog buffer configurable, we propose a biasing current source that can be configured to four fixed values from 2 mA up to a maximum of 16 mA. The needed slew-rates were selected in a linear fashion as shown in Figure 4.9.

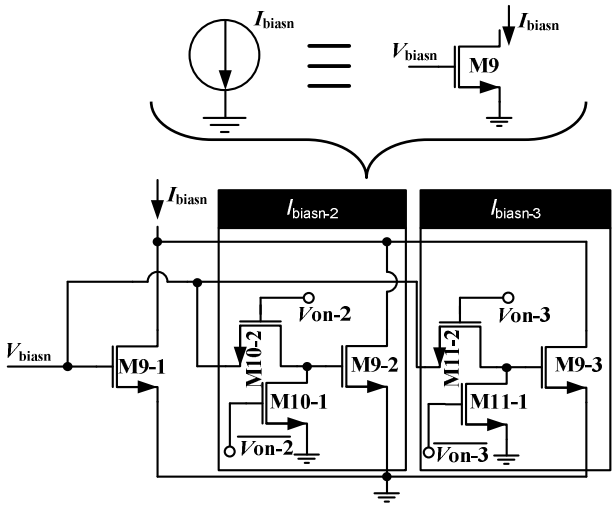


Figure 4.8 Proposed slew-rates with a two bits configuration.

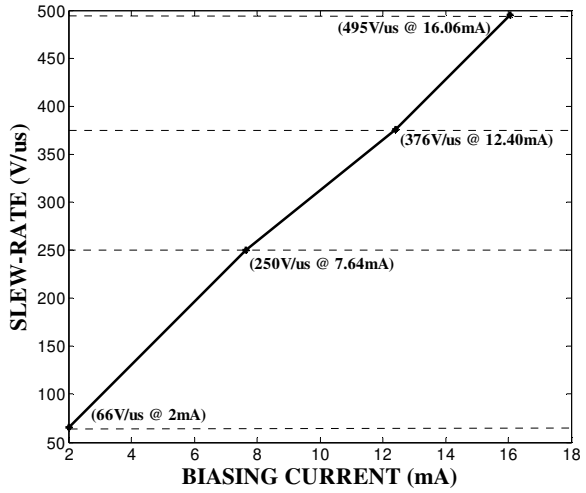


Figure 4.9 Proposed biasing current and slew-rates configuration for the complementary CMOS analog buffer.

4.3.4 Results and Performance Analysis

The proposed configurable analog buffer has been experimentally validated through post-layout simulations performed in a 0.18 µm CMOS technology. As stated in the introduction section, the WaferIC benefits from an architecture where no metal line are needed to connect the NanoPad to the uIC ball, which drop the overall parasitic capacitance to around 8 pF. For that reason, the following simulations results were extracted with a load of 12 pF.

4.3.4.1 Transient response, slew-rate configuration and output voltage swing

To depict the performances of proposed configurable analog buffer proposed in Figure 4.5, transient analysis were done. The worst case scenario of a 25 MHz square wave signal was applied to v_{in} with rising and falling slopes of 500 ps at a maximal amplitude 3.3 V_{PP}. Post-layout simulations shown in Figure 4.10 were done throughout all configurable slew-rates, which vary from 66 V/µs, at a biasing current of 2.00 mA, up to 495 V/µs, for a 16.06 mA biasing current.

The output swing follows the theoretical analysis given in section III, where V_{DSAT} is to set the maximum and minimum output voltage swing of the proposed buffer. Figure 4.10 shows that for I_{biasn} of 2.00 mA, V_{DSATp} is at its lowest with 150 mV. This value increases linearly with I_{biasn} as shown in Figure 4.11and reaches a maximum of 490 mV at maximum slew-rate as the theoretical analysis predicted it (when I_{biasn} increases so is V_{DSAT}). The output voltage swing is thus a linear relation with the slew-rate. Detailed results are displayed in Tableau 4.1.

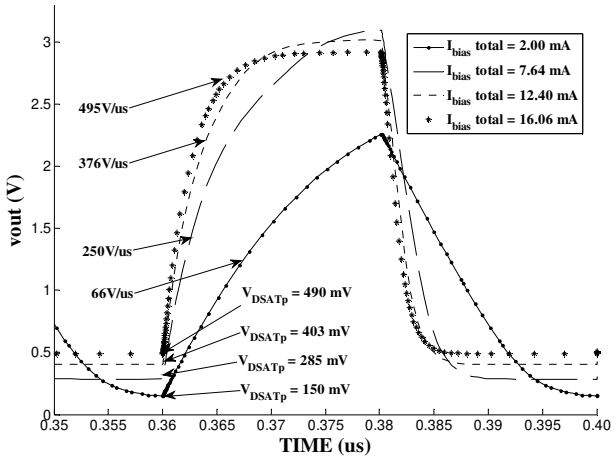


Figure 4.10 Output voltage transient response to a 25 MHz square wave of the proposed output buffer with 4 different configurable slew-rates for a 12 pF load.

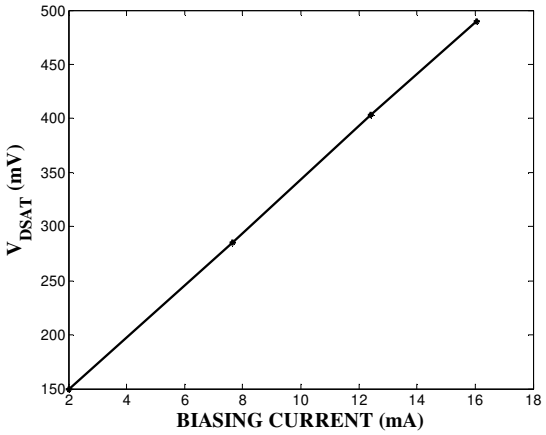


Figure 4.11 Relation between biasing current and V_{DSAT}, which set the maximum output voltage swing.

4.3.4.2 AC characterization, power-supply-rejection-ratio and output distortion

The AC response of the proposed analog buffer can be seen in Figure 4.12. All configurable outputs confirm what (4) was predicting a voltage gain close to unity. As a result of the choice of topology and the sizing of transistor, the assumption of $gm_3 \cdot rds_2 // rds_4 >> 1$ can be made, making (4) close to unity. The gain (A_v) is -121 mdB at 66 V/µs and decreases to a minimum of -355 mdB at maximum slew-rate of 495 V/µs. Figure 4.12 shows that all the configurations of the analog buffer have a constant gain for the entire operating bandwidth (no ripples). This constant gain ranges from 4.0 MHz (at 66 V/µs) and goes up to ten times more, 40 MHz (495 V/µs). Figure 4.12 also shows the -3 dB cut-off frequency, where the minimum and maximum bandwidths are 74 MHz and 194 MHz.

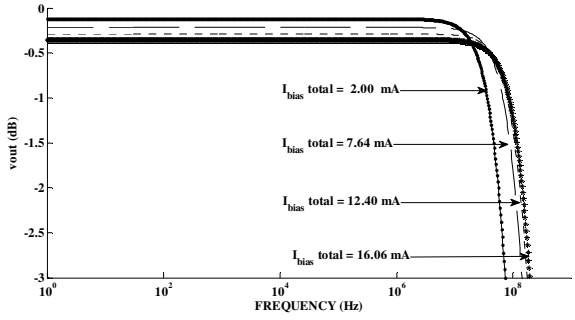


Figure 4.12 AC response of the proposed analog buffer for the four configurable slew-rates with a load of 12 pF.

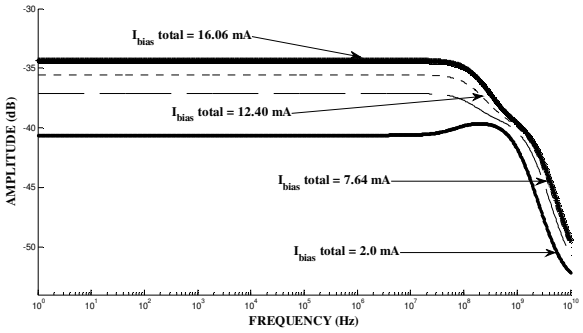


Figure 4.13 PSRR of the proposed analog buffer for the four configurable slew-rates with a load of 12 pF.

Tableau 4.1 Performance summary of the proposed configurable analog buffer

	Config. 1	**Config. 2**	**Config. 3**	**Config. 4**
I_{bias} **(mA)**	2.00	7.64	12.40	16.06
Slew-Rate (V/µs)	**66**	**250**	**376**	**495**
V_{DSATp} **(mV)**	150	285	403	490
V_{DSATn} **(mV)**	100	200	290	382
Output Swing (V)	3.05	2.815	2.607	2.428
Gain (mdB)	**-121**	**-216**	**-289**	**-355**
PSRR @ 0 Hz (dB)	-40.6	-37.1	-35.5	-35
PSRR @1 MHz (dB)	-40.6	-37.1	-35.5	-35
PSRR @100 MHz (dB)	-39.8	-37.7	-36.1	-35
Settling Time (ns)	142	11.8	7.2	5.
-3 dB bandwidth (MHz)	**74**	**143**	**176**	**194**

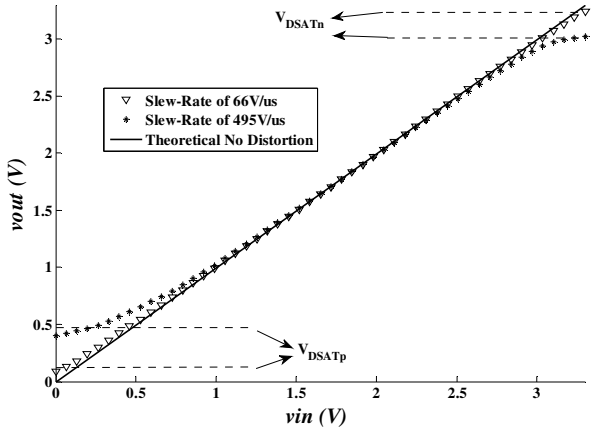


Figure 4.14 DC transfer function for minimum and maximum slew-rate configuration compared to the theoretical no-distortion linear output.

We explained in section III that the WaferIC will suffer from noisy power-supply lines. Taking this into account, any circuit using these power supplies has to be as independent as possible from them. The power supply rejection ratio (PSRR) is shown in Figure 4.13. The simulations results show that the proposed analog buffer is insensitive from DC to high-frequency noise coming from the power supplies. The low-frequency noise is rejected with more than 40 dB at low I_{bias} = 2 mA (or the smallest slew-rate), and still performs adequately with a -35 dB of PSRR with the largest bias current.. A small ripple can be observed around 100 MHz, which is compensated by the load itself. Figure 4.14depicts DC transfer function for a voltage input that ranges from 0 up to 3.3 V for minimum and maximum slew-rate. As the simulations shows when operating at small slew-rate, the amplitude distortion is minimal as the DC transfer function is almost linear.

The main performances criteria are listed and compared in Tableau 4.1 for all four configurations. The settling time was calculated at 90 % of maximum output swing for a square wave input of 25 MHz as shown in Figure 4.10.

Tableau 4.2 presents a performance comparison between existing works and our proposed configurable analog buffer. In order to adequately compare two architectures with different targets and applications regarding operating speed, load and silicon area, a figure of merit (*FOM*) is describe in (6), where the Normalized Area (NA) to 0.18 µm is calculated for a more accurate silicon comparison, the Settling Time (ST) the Load the Voltage Gain (A_V) and the Slew-Rate

(*SR*) are the parameters taken into account. The smaller the *FOM* the better the buffer gets. Our proposed configurable analog buffer has a FOM more than 120 times lower than that of a rail-to-rail class-AB CMOS buffer introduced [12]. This factor is mainly due to the very high slew-rate capabilities of the proposed solution.

$$FOM = \frac{NAgST}{Load\,gAvgSR} \qquad (6)$$

Tableau 4.2 Comparison with existing works

	[10]	[12]	**This Work**
Year	2004	2012	2013
Technology (µm)	0.35	0.35	0.18
Power Supply (V)	3.3	3.0	3.3
Transistor count	26 and R=2k	20	21
Active area (mm^2)	0.00265	0.01460	0.001824
Load (pF)	600	20	12
Gain (dB)	0	0	-0.121 to -0.355
Settling time (ns)	2700	87 ns for a 3 V square wave	5.3 ns for a 3.3 V square wave
Slew-Rate (V/µs)	4.52	81	66 up to 495
-3 dB bandwidth (MHz)	-	5.8	74 to 194
FOM	0.697	0.207	0.00169

4.3.5 Conclusion

A novel approach using complementary nMOS and pMOS stages architecture of modified differential pairs for a configurable analog buffer has been presented. The introduced buffer can

be set to various slew-rates from 66 up to 495 V/µs to suit wafer-scale integration prototyping platform, the WaferIC, where power-supply noise injection and available silicon area are an issue. The proposed analog buffer used only 21 transistors for a total silicon area of 0.001824 mm^2. In addition, the proposed analog buffer has a quasi-unity gain and fast response with a bandwidth that goes up to 194 MHz and a response time of 5.3 ns. This design also achieves a *FOM* better than other designs by a factor of more than 120 times.

CHAPITRE 5 CONCEPTION D'UN RÉSEAU DE CONVERTISSEURS CNA TOLÉRANT AUX PANNES DÉDIÉ À L'INTÉGRATION À LARGE ÉCHELLE

5.1 Résumé

Le chapitre précédent propose un tampon analogique utilisé au bout de la chaîne lors de la transmission d'un signal analogique d'un NanoPad à un autre. Ce chapitre se concentre sur la conversion dans le domaine numérique effectuée par le NanoPad échantillonnant le signal analogique ainsi que sur la conversion dans le domaine analogique, effectuée avant le tampon analogique, par le NanoPad récepteur.

La surface de silicium disponible étant très limitée, un réseau de CAN et de CNA où l'accès à ceux-ci est partagé entre tous les NanoPads est proposé. Ce réseau inclus 2 CAN et 2 CNA par Cellule pour un total de 311 296 convertisseurs. Chaque NanoPad possède un accès privilégié à un CAN et un CNA mais peut, en cas de défectuosité du WaferIC, avoir accès aux convertisseurs de n'importe quelle Cellule dans son plan horizontal, ou en d'autres termes aux convertisseurs EST ou OUEST.

L'article « *A Defect-Tolerant Reusable Network of DACs for Wafer-Scale Integretaion* » a été soumis à la revue de journal « *IEEE Transactions on Very Large Scale Integration* » le 13 septembre 2017. Cet article propose une approche nouvelle et originale pour un CNA. Ce dernier, également utilisé dans le WaferIC comme référence de tension configurable, se base sur une paire différentielle modifiée pour étendre une tension de référence générée par un « *bandgap* » sur une très grande plage de valeurs. Ce CNA est réutilisé pour concevoir un CAN de type « *SAR-ADC* » et un réseau de plus de 300 k convertisseurs est proposé ainsi qu'un système pouvant pallier aux pannes et aux défectuosités du WaferIC. Le CNA proposé peut être configuré de 850 mV jusqu'à 2.538 V avec une résolution de 8-bits et un nombre effectif de bits de 7.6. Une méthode de calibration y est également proposée où un ajustement fin de toute la plage de tension peut être effectué sur une plage d'environ 25 mV. Le taux de conversion du CNA est de plus de 10 MS/s et affiche une surface de silicium ultra compacte de 0.00035 mm^2.

5.2 Contribution au domaine scientifique

La contribution majeure de cet article est la proposition d'une approche tout à fait nouvelle et innovatrice pour concevoir un CNA. Cette technique permet de concevoir un convertisseur dans une surface de silicium compacte et peut être adaptée à n'importe quelle tension de référence et plage de valeur. De plus, une technique de calibration permet un ajustement précis du CNA en question. Une seconde contribution est l'implémentation d'un réseau de CAN-CNA au niveau WaferIC permettant la transmission de signaux analogiques en plus d'être tolérant aux pannes.

5.3 Article # 3 : A Defect-Tolerant Reusable Network of DACs for Wafer-Scale Integration

Abstract— A novel defect-tolerant network of Digital-to-Analog Converters (DACs) is presented in this paper. The architecture of this converter employs a single 2.5 V voltage reference and an unbalanced buffering technique to achieve a wide voltage range that extends from 864 mV to 2.538 V with an 8-bit resolution. The proposed converter incorporates a defect-tolerant architecture and is extremely compact, utilizing a per-bit silicon area of less than 350 μm^2. Although such very small area allows for embedding in dense configurable fabrics (FPGAs) and wafer-scale integration, the overall performance is not sacrificed as reported measurements show a signal-to-noise ratio of 51.87 dB and a spurious free dynamic range of 42.31 dB, at 10 MS/sec providing 7.6 effective bits. Moreover, the proposed architecture benefits from dynamic calibration capabilities, as any converter output can be finely adjusted over a range of 25 mV. This proposed DAC is also extensively reused in the same defect-tolerant network as for a SAR-ADC, as well as a configurable voltage reference.

5.3.1 INTRODUCTION

Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) are important and even critical components in current electronic designs. They are among the key building blocks that bridge analog and digital circuits. With today's increasing use of mobile devices, there is a growing demand for access to low-cost, low-power, and high-performance ADCs and DACs [1]. Indeed, they are used for carrying out different kinds of data conversions in many types of applications, such as noise rejection, data sampling, power consumption monitoring and biomedical applications [2].

The novel WaferIC prototyping platform introduced in [2] [3] is a good example of a complex electronic system requiring numerous ADCs and DACs. This wafer-scale circuit behaves like a configurable printed circuit board (PCB) that extends over the full surface of a 200 mm silicon wafer (see Figure 5.1) [3] [4].

ADC Topologies

Several different topologies exist for both ADCs and DACs. Four main techniques to designing ADCs are reported in the literature : *flash, pipeline, successive approximation* and *sigma-delta* (oversampling) [5]. The various approaches can be quantified with a few parameters, such as the resolution (number of bits), the signal-to-noise ratio (SNR), the spurious-free dynamic range (SFDR), the power dissipation and the effective number of bits (ENOB) [5]. We will briefly describe the types of architectures that are currently used for designing ADCs.

The *flash* architecture is parallel in nature, and is considered to be the fastest. Nevertheless, it uses 2^{N-1} comparators, where N is the resolution. Because the number of comparators grows exponentially with N, this approach is not energy efficient and employs a very large silicon area, thus making it unusable for wafer-scale integration or embedding in dense configurable fabrics such as FPGAs. Moreover, the numerous integrated components, such as resistor-ladders, make layout matching challenging and have limited this approach to building ADCs having up to only N=9 bits of resolution [5] [6].

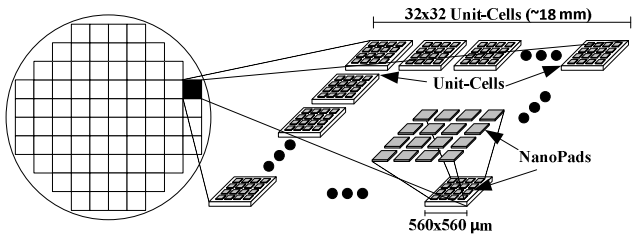


Figure 5.1 The WaferIC is composed of a same 32×32 matrix of Unit-Cell that is photo-repeated 76 times over the surface of the whole wafer.

The *pipeline* ADC architecture is mostly used in high-speed applications, such as wideband receivers, where the power consumption is to be considered [7]. Pipeline ADCs are often implemented using switched-capacitor circuits, and their overall performance depends on the required operational amplifiers (op-amps) and the size of the capacitors used : the larger they are, the better the matching can be, but this is done at the expense of an increase in power consumption and silicon area [7]. The integration of such numerous large capacitances also makes this approach unsuitable for use in the WaferIC.

The *delta-sigma (ΔΣ)* architecture uses digital circuit blocks instead of analog ones, and trades speed for overall resolution by sampling the input signal at a rate several times larger than the Nyquist rate [5]. Switched capacitor networks are widely used as building blocks for the architecture, which makes the ΔΣ-ADC larger to integrate [8]. A solution minimizing the number of integrated passive components and offering signal integrity over large silicon distances (full 200mm wafer) is necessary for use with the WaferIC, thus excluding the ΔΣ-ADC architecture as a viable option.

The authors in [9] explored a solution using an asynchronous delta-modulator based architecture as a solution. This proposed approach is however targeted for a moderate bandwidth of 2 MHz.

Successive Approximation Register (SAR) based ADCs have a small silicon area footprint and a low-power consumption, since, compared to the other approaches, the converter only requires a single signal path with one comparator. It offers a high resolution in exchange of conversion speed. The total conversion cycle is spread over several clock cycles, in which the input signal is compared with a reference level delivered by a DAC [6]. A SAR-ADC is composed of three distinct modules (Figure 5.2). The first module is a digital controller, which asserts the second module, a DAC. The third module is a comparator that generates a *Trigger* signal after determining whether the input V_{IN} (signal to sample) is equal to the value produced by the DAC

[23], [26], [28]. The size and performance of the SAR-ADC mostly depends on the switched capacitor or current steering DAC employed [23].

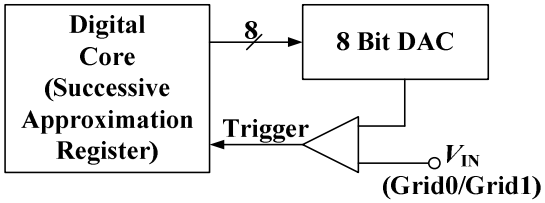


Figure 5.2 Typical SAR-ADC architecture.

5.3.2 DAC Topologies

Digital-to-analog converters are typically based on either *current-steering*, a *charge scaling technique* or a *resistive ladder*. The *current-steering* topology requires a large number of distinct and matched current sources, which significantly impacts the resulting silicon area. Indeed, as shown in [11], the required silicon area for a binary-weighted current steering 10 bits DAC is 4 times larger than the available surface for a full NanoPad. Other designs have been published in [12] and [13], but none have a silicon area comparable to or less than that of a NanoPad.

The *charge scaling technique* requires a large number of integrated passive components that need to be matched. None of the published topologies offer a small-enough silicon area such that it could be used for wafer-scale integration into the WaferIC [14], [15].

Since the WaferIC integrates over 1.2 million NanoPads, and each NanoPad has to be able to access both ADC and DAC functionalities, a large number of integrated converters is required. To the best of our knowledge, no existing design or topology allow for wafer-scale integration within the silicon area and power budget available on the targeted platform.

In this paper, a SAR-ADC architecture is proposed. It employs a novel DAC based on an unbalanced buffering technique. The DAC does not require switched capacitors or current steering techniques, and only uses a single 2.5 V voltage reference to generate 256 different voltage levels. Using this novel architecture, 300 thousand of these ADCs/DACs can be integrated into a defect-tolerant network that is suitable for wafer-scale integration. The addition of ADCs and DACs to a platform such as the WaferIC enables support for a wider range of applications, such as internal/external signal sampling, analog signal generation, and interfacing

with analog busses. Furthermore, it allows for processing and generating analog signals, sampling, and providing analog bus functionality.

In order for this addition to be effective, ADCs and DACs have to be accessible from each and every one of the 1.2 M NanoPads, which is a challenge in terms of minimizing the total resulting silicon area. Moreover, wafer-scale integration requires the use of redundancy and defect-tolerant architectures since no fabrication process has a yield of 100%, particularly at that level of integration. Therefore, we propose the use of a defect-tolerant network of ADCs and DACs: over 300 thousand converters are shared between all NanoPads. The proposed ADCs/DACs are based on an unbalanced buffering technique that yields a very compact silicon area. Combined with the proposed sharing network, they allow for any defects to be overcome by re-routing the faulty ADC/DAC functionalities to a working set of ADCs/DACs. The same DACs are also employed in the ADC structure, and their per-bit silicon size of 350 μm^2 does not compromise performance. Indeed, at 10 MS/s, SFDR of 41.31dB and an ENOB of 7.6 bits were measured.

The paper is organized as follows : Section II focuses on the proposed small-area DACs, which are also employed in the proposed Successive Approximation Register based ADCs (SAR-ADCs). The implemented defect-tolerant ADC/DAC network is described in Section III. In Section IV, experimental results obtained from a test chip implemented using 0.18µm CMOS technology are reported, and in Section V the proposed solution is compared with other recently published ADC/DAC architectures.

5.3.3 A DAC Architecture Based on Unbalanced Buffer

Conventional DAC structures mainly employ switched capacitor networks or current steering techniques. Integrating and matching a large number of either capacitances, current sources or other passive components has a large impact on the silicon area, and thus determines whether they can be integrated within the WaferIC or not.

In this section the proposed DAC is presented. This circuit is adapted from the analog buffer in [18]. The characteristics of an implemented solution are reported and means to maximize the output range while minimizing the silicon area are explored.

5.3.4 A multi-reference voltage-level generator

The three-stage circuit presented in [18] (see Figure 5.2) employs a configurable unbalanced differential pair for generating a range of output voltages. The first stage of this circuit uses a conventional bandgap generator (BGR) to provide a stable 1.5 V reference voltage that is insensitive to temperature and power-supply variations. The second stage employs this single voltage reference to generate a range of 246 distinct voltage levels, each at around a 10 mV step increment. This is achieved by selecting the transistor ratios in the unbalanced differential pair in order to shift the reference voltage up or down. In the third stage the generated output voltage from the second stage is buffered, to allow driving a larger load at V_{OUT} (see Figure 5.3). From [17] the expression of V_{OUT} is given by (1)

$$V_{OUT} \propto \sqrt{W_3 L_4 / W_4 L_3} \qquad (1)$$

If we were to vary both M3 and M4 to widen the unbalancing capabilities, offsetting the 1.5V reference both down and up equally, this approach would be plagued by the non-monotonous output voltage V_{OUT}. It would require the use of a digital decoder where the digital '0' would be 1.5V, '-128' the lowest value such as '1.5V-*X*mV' and '+128' the highest value at '1.5V+*X*mV'. The approach used in [17] sets M3 ratio (*W/L*) down to achieve lower output voltages of that the voltage reference of 1.5V. Then M4 ratio is scale up properly to increase V_{OUT} from 1.33V(digital 0) up to 3.04V (digital 256). M3 could be scale down deeper to achieve lower value at the cost of a large increase of M4 silicon area.

5.3.5 Proposed unbalanced buffer

When speaking of Wafer Scale integration, such as in the WaferIC, the used silicon area is one of the foremost criteria. Using circuits that can be reused several times or reconfigured to achieve different functionalities is crucial. The proposed unbalanced buffer is a structured intended to be used as an 1:1 analog buffer, a DAC, a SAR-ADC, and a configurable voltage reference. We will focus in this paper on its capabilities of a DAC, and a voltage configurable voltage reference.

In this paper, a novel approach is proposed for improving the multi-stage level generator shown in Figure 5.3. Indeed, it employs a similar approach as that of [17] by combining it with the configurable and compact analog buffer presented in [18] (Stage #3), and enhances it to eliminate its non-monotonic nature and combines it with Stage #2, thus increasing its driving capability and its output voltage range.

The analog buffer in [18] uses a modified differential pair comprising complementary nMOS and pMOS stages to achieve a wide output range. Figure 5.4 shows a transistor-level schematic of this buffer. M1 and M2 form a simple current mirror while M3 and M4 are the modified differential pair. When M1 has the same size as M2, and M3 has the same size as M4, if we neglect the channel modulation and assume that all transistors are in their saturation region, I_1 and I_2 can be approximated by (2) and (3) respectively :

$$I_1 = \frac{\beta_3}{2}\left(V_{IN} - V_2 - V_{THN}\right)^2 \qquad (2)$$

$$I_2 = \frac{\beta_4}{2}\left(V_{OUT} - V_2 - V_{THN}\right)^2 \qquad (3)$$

where β_X is the transconductance parameter of transistor x. Note that when the circuit in Figure 5.4 is balanced, $\beta_1 = \beta_2$ and $\beta_3 = \beta_4$, thus $V_{OUT} = V_{IN}$.

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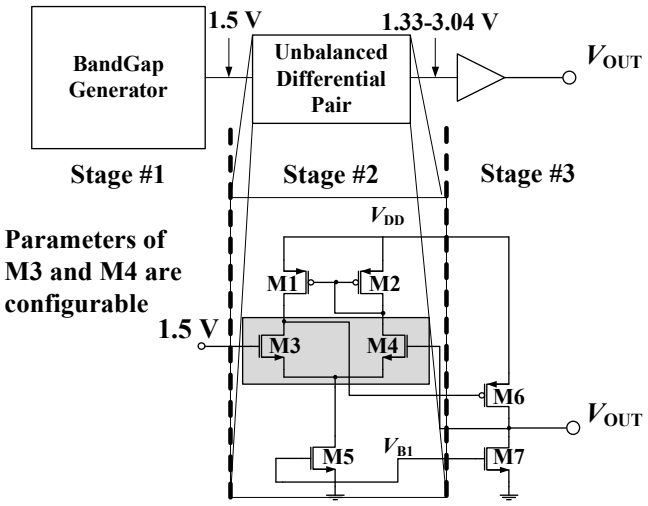

Figure 5.3 Unbalanced differential pair using a single 1.5 V voltage reference to generate 246 output voltages at 10 mV step-intervals, ranging from 1.33 to 3.04 V [17].

The circuit in [18] was modified to employ an enhanced unbalanced circuit as of in [17]. Indeed, the resulting circuit implements an ultra-compact 8-bit DAC (Figure 5.4). Note that V_{OUT} depends on I_1 and I_2, which are approximated by (4) and (5) as follows :

$$I_1 = \frac{\beta_1}{2}\left(V_{DD} - V_1 - V_{THP}\right)^2 \qquad (4)$$

$$I_2 = \frac{\beta_2}{2}\left(V_{DD} - V_1 - V_{THP}\right)^2 \qquad (5)$$

Therefore, neglecting the channel modulation, the value of V_{OUT} can be approximated by first equaling (2) to (4) and (3) to (5), such as to isolate V_1 as shown by (6) and (7) below.

$$V_1 = \sqrt{\frac{\beta_3}{\beta_1}}\left(V_{IN} - V_2 - V_{THN}\right) + V_{DD} + V_{THP} \qquad (6)$$

$$V_1 = \sqrt{\frac{\beta_4}{\beta_2}}\left(V_{OUT} - V_2 - V_{THN}\right) + V_{DD} + V_{THP} \qquad (7)$$

Then, assuming all transistors are in saturation region and that transistors M3 and M4 have an equal size (i.e. $\beta_3 = \beta_4$), by equaling (6) to (7) and isolating V_{OUT}, (8) can be obtained.

$$V_{OUT} = \sqrt{\frac{\beta_2}{\beta_1}} V_{IN} + \left(1 - \sqrt{\frac{\beta_2}{\beta_1}}\right)(V_2 + V_{THN}) \qquad (8)$$

Nevertheless, as the V_{OUT} voltage increases, depending on the size of M2, V_{DS2} may fall below the value of V_{DSAT}, the voltage necessary for M2 to remain in the saturation region, thus placing the transistor in its triode region. The current flowing through M2 would then be given by (9), and V_{OUT} can then be approximated by (10) below.

$$I_2 = \beta_2 (V_1 - V_{DD} - V_{THP})(V_1 - V_{DD}) - \frac{(V_1 - V_{DD})^2}{2} \qquad (9)$$

$$V_{OUT} = \sqrt{\frac{2\beta_2}{\beta_4}} \sqrt{\frac{\beta_3}{\beta_1}(V_{IN} - V_2 - V_{THN})^2 - \sqrt{\frac{\beta_3}{\beta_1}}(V_{IN} - V_2 - V_{THN} - V_{THP})^2} \qquad (10)$$
$$\ldots + V_2 + V_{THN}$$

Equations (8) and (10) reveal the V_{OUT} dependency on all transconductances β_x, thus allowing several degrees of freedom for unbalancing and configuring the output voltage. Indeed, by looking at (8) and (10), the common βx terms in both equations would be β_1 and β_2 (since β_3 only appears in (10)). Using variables β_1 and β_2 to configure the circuit would make the design simpler, since V_{OUT} can then be expressed using a common set of terms for (8) and (10). Increasing the width of M1 would result in an increase of β_1, thus resulting in a lower V_{OUT}. Increasing its length would result in the opposite effect (i.e. an increased V_{OUT}). Conversely, varying the width and length of M2 would have a complementary effect. However, only β_2 is present in (8) and (10) with the same exponent (i.e. $\beta_2^{(1/2)}$) and therefore using it (instead of β_1)

for configuring the circuit greatly simplifies the transistor size selection, thus allowing for a more regular growth of the resulting V_{OUT}. Nevertheless, selecting M2 as the transistor for unbalancing the circuit allows several scenarios. Some of these scenarios may improve the voltage range, while others may reduce the silicon area, or the number of necessary reference voltages (V_{IN}).

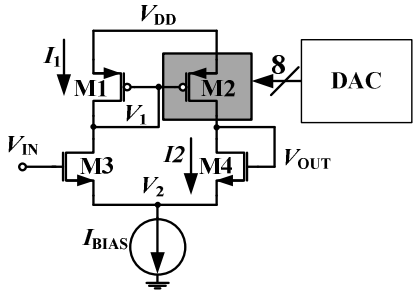

Figure 5.4 The simplified schematic of the 8-bit configurable analog buffer based on [18], and which replaces Stages 2 and 3 in Figure 5.3.

5.3.6 Proposed technique to set the overall output range

In wafer-scale integration, particularly for the WaferIC, the most important criteria for selecting a design over another is the silicon area employed and the maximum output voltage range achieved. Indeed, the objectives are to minimize the *silicon area* and *maximize the output voltage range*. To that end, different possible scenarios for obtaining a compact yet flexible DAC are considered.

When using the proposed buffer-unbalancing technique, the appropriate V_{IN} reference voltage and an effective output range must be selected. Ideally, transistors M1 to M4 in Figure 5.4 should always be in saturation to ensure that (9) remains valid. Therefore, M3 and M4 must be equal in size, leaving M1 and M2 to be adjusted and configured. Recall that as M1 is sized larger than M2 (i.e. $\beta_1 > \beta_2$), V_{OUT} decreases. Conversely, as M1 is sized smaller than M2, V_{OUT} increases.

Four scenarios are proposed, each providing a different output linearity, output voltage range and silicon area usage.

In the first scenario, V_{IN} is initially chosen such that it is equal to the center value of the expected output voltage range. Then, by resizing both M1 and M2, the value of V_{OUT} can be configured down to V_L (voltage low) or up to V_H (voltage high). Indeed, whereas increasing the width of M1 moves V_{OUT} toward V_L, increasing the width of M2 moves V_{OUT} toward V_H. Finally,

when both M1 and M2 are equal in size, $V_{OUT} = V_{IN}$. However, to ensure its monotonicity, a digital encoder is required as in [17] and detailed in section II(a). Another approach of the one used in [34] is proposed. To increase V_{OUT} higher than V_{IN}, M2 ratio (W/L) needs to increase while keeping M1 ratio constant, or the other way around to make V_{OUT} lower. In a 8-bits configuration the logical '0' would be when $V_{OUT}=V_{IN}$. Then the 4-LSB (Least Significant Bit) would move V_{OUT} toward its minimum value reaching it at the digital code "1111". To increase $V_{OUT} > V_{IN}$ the 4-MSB would then be used while maintaining the 4-LSB at "0000". This approach severely impacts the required number of bits since 8-bits would give and overall 64 different V_{OUT} as well as needing also a digital decoder. Doing otherwise would negate the monotonicity where several voltage intervals would interlace with one another.

The second scenario, consists in employing a fixed V_{IN} value, locked at V_L or either V_H. In this case, the full output voltage range is obtained by resizing M2 up or down to range V_{IN} up or down depending on the designer's choice. A lower V_{IN} value may be attained by using a low-voltage BGR, or by fixing the size of M1 to a larger value.

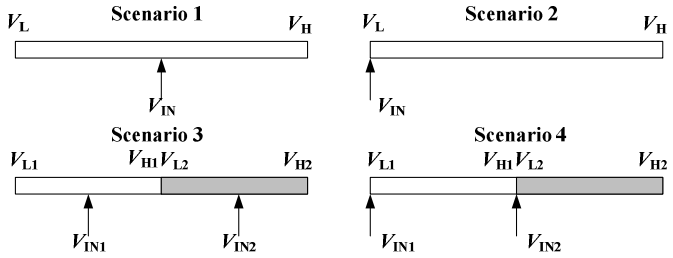

Figure 5.5 Proposed scenarios to range a single V_{IN} into several V_{OUT}.

Scenarios 3 and 4 are similar to Scenarios 1 and 2, but use two V_{IN} values rather than one fixed V_{IN}. The output range for each V_{IN} and the overall configurable size of M1 and M2 are then reduced. The advantage offered by Scenarios 3 and 4 is that smaller M1 and M2 transistors can be used to obtain the same overall V_{OUT} voltage range. Nevertheless, this is achieved at the expense of having to generate multiple references, which is costly in terms of silicon area. Moreover, this approach makes the monotonicity hard to achieve when switching from one reference to another while keeping the step sizes small and constant. It would require very precise voltage references as well as very small offsets.

Tableau 5.1 summarizes and compares the main characteristics of the four proposed scenarios. As can be seen, Scenarios 3 and 4 require multiple V_{IN} references, each generated from a different BGR, which typically require parasitic PNP transistors having prohibitively large silicon areas. We can also observe that Scenario 1 may be unsuitable and is not the best in the target application as its monotonicity would required a digital decoder as well as only offering 64 V_{OUT} with an 8-bit configuration. Therefore, given that *minimizing the silicon area* and *maximizing the output voltage range* main selection criteria, Scenario 2 was chosen for implementing the DAC. The non-linear output voltage range observed for Scenario 2 is not as critical, given that the DAC is to be used in SAR-ADC solution. Indeed, this non-linearity is compensated in an analog bus (ADC to DAC), since the same DAC would be used for the input (i.e. data sampling) and the outputs. Moreover, since the transfer function of the proposed DAC is known, (see (8) and (10)), it is possible for the user to linearize the output when necessary. The key message to remember is that while the chosen design, Scenario 2, offers a monotonic output voltage range and only involves a single reference voltage, its full range of generated output voltages is not linear.

The effective width of M2 can be adjusted by varying its 8-bit digital input code (see Figure 5.4). Figure 5.6 depicts the simulated V_{OUT}, as a function of (8) and (10), for different widths of transistor M2 and a fixed M1 transistor width. Each plotted line represents a per-bit width of M2, chosen as a multiple of a factor K (where K is an integer ranging from 1 to 255) with the minimal transistor width U. Thus, for each digital input code bit-increase, the effective width of M2 grows by $K \cdot U$. Figure 5.6 also shows the overall output voltage linearity obtained with the proposed technique. As can be observed, the more M1 and M2 are unbalanced, that is, the more different their widths are, the less linear the full output voltage range becomes.

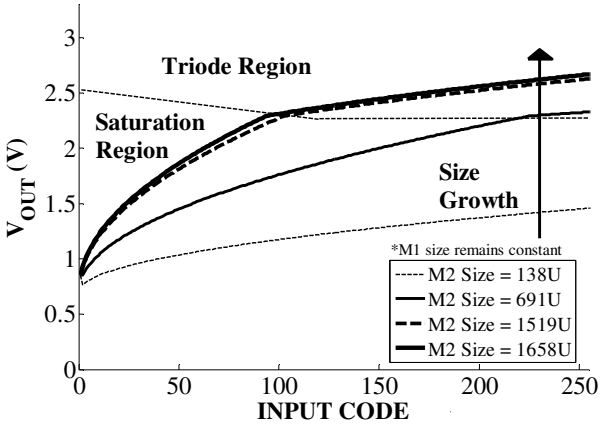

Figure 5.6 Simulated DAC voltage as a function of its digital input code, for different widths of M2 and while employing a single BGR voltage reference.

Tableau 5.1 Comparison of the 4 proposed scenarios.

	Scenario 1	**Scenario 2**	**Scenario 3**	**Scenario 4**
M1 and M2 Sizes	Medium	Large	Small	Medium
# of V_{IN} References	1	1	2	2
Overall Silicon Area	Large	Medium	Large	Large
Monotonicity	YES (with decoder)	YES	NO	YES
Linearity on the full V_{OUT} range	NO	NO	YES	YES

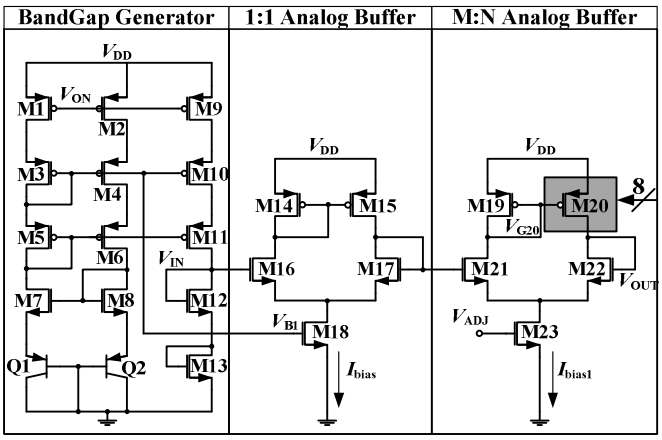

Figure 5.7 Proposed solution for generating analog voltages using an unbalanced buffer technique.

5.3.7 Proposed DAC using the unbalanced buffer technique

The proposed circuit shown in Figure 5.7 includes 3 distinct stages. The first stage is a BGR, the second is a 1:1 analog buffer, and the third is the proposed unbalanced buffer (Figure 5.7).

The BGR is adapted from [17]. A Proportional To Absolute Temperature (PTAT) current is created through M3 and M8, and then it is duplicated by M10 and M11. A cascode current mirror was chosen to obtain a better V_{DD} noise isolation. The PTAT current is then pushed into diode-connected transistors M12 and M13, which are Complementary To Absolute Temperature (CTAT).

Transistors M1, M2 and M9 are on/off switches controlled by V_{ON} to enable or disable the circuit. Proper current management is important in wafer-scale integration : since the proposed wafer-scale circuit is populated with over 300k ADCs and DACs, their currents quickly add up. For example, if all 300k ADCs and DACs were always kept on, a quiescent current of 100 µA per circuit would result in a total of 30 A of potentially wasted current. Therefore, having the ability of independently turning specific circuits on and off is mandatory.

The expression for V_{IN} is given by (11). Assuming both drain currents are equal (i.e. $I_{D12} = I_{D13}$) (12) can be obtained. The temperature behavior for each term in (12) is express in (13). By properly adjusting I_{D12}, V_{IN} can become insensitive in the first order to temperature variations.

$$V_{IN} = V_{GS13} + V_{GS12} = \sqrt{\frac{2I_{D13}}{\beta_{13}}} + \sqrt{\frac{2I_{D12}}{\beta_{12}}} + 2V_{THN} \qquad (11)$$

$$V_{IN} = 2V_{THN} + \sqrt{2I_{D12}}\left(\frac{1}{\sqrt{\beta_{13}}} + \frac{1}{\sqrt{\beta_{12}}}\right) \qquad (12)$$

$$V_{IN} \propto \text{CTAT+PTAT} \qquad (13)$$

The 1:1 analog buffer in the second stage shields the bandgap generator from the M:N analog buffer. Indeed, the 8-bit addressable transistor M20 can inject noise on the gate of M21. The BGR in the first stage is not designed to sustain this type of noise, nor is it designed to drive a large current. The use of this buffer isolates the first and third stages, and ensures that the proposed DAC in the third stage remains stable and able to offer a high-bandwidth.

In order to obtain a 1:1 analog buffer that is insensitive to temperature variations, I_{BIAS} needs to be CTAT (see Figure 5.7). The electron mobility of a transistor decreases as the temperature increases, thus decreasing the drain current of a transistor. In counterpart, the threshold voltage (V_{TH}) has a CTAT effect on the current : at lower V_{GS} as the transistor mobility effect dominates, making the overall drain current PTAT; the opposite occurs at higher V_{GS}, making the drain current CTAT [18]. By using M18 as a bias current source with its gate connected to V_{B1}, the I_{D18} current is ensured to be CTAT since its V_{GS18} remains at a higher voltage (~2.5 V), thus helping the 1:1 analog buffer to achieve temperature independence. V_{IN} has been set to an output voltage of 2.5 V and will be varied down to ~850 mV, as per Figure 5.6.

The final stage is the configurable M:N analog buffer. Only transistor M20 is configurable in size, such as to lessen the silicon area requirements. Scenario 2 was selected (see Figure 5.5), to reduce V_L down to 0.85V from the 2.5 V BGR generated voltage (V_{IN}). Indeed, the size of M19 size was chosen such that this targeted lower voltage value could be reached. Using this technique, the chosen M1 and M2 sizes allow V_{IN} to be varied from 0.85 V to 2.5 V with an 8-bit resolution (maximum range). The widths of the 8 transistors constituting M20 range from a minimum-sized transistor width in the 0.18µm CMOS technology employed (i.e.

$W_{MIN} = 0.42\ \mu m$) to a maximum width of $128 \times W_{MIN}$, using a quadratic growth for each addressable bit (i.e. a doubling of the width for every additional addressable transistor). The result is a linear increase of M20's size from W_{MIN} to $256 \times W_{MIN}$ with W_{MIN} steps.

To mitigate process variation effects and to improve the matching between pairs of ADC-DAC converters in the WaferIC, a dynamic calibration method is also proposed. The DAC's bias current can be adjusted using the V_{ADJ} signal at the gate of M23 (see Figure 5.7), thus varying the V_{OUT} output voltage up or down as required. Using this method, the circuit can compensate for process variations, mismatches, and even temperature or V_{DD} variations, since V_{OUT} depends on I_{BIAS1} as demonstrated in (9).

The aim of this paper, as mentioned in previous sections, is to reused the proposed configurable analog buffer as a DAC, a configurable voltage reference, as part of a SAR-ADC and as a 1:1 analog buffer. Thus the calibration of V_{ADJ} would be done by a neighboring DAC used as a configurable voltage reference. The setting of V_{ADJ} within the WaferIC could be done using its contact detection mechanism [4], where a pull-up of 1.8V can be applied at any NanoPad. Using this known reference, V_{ADJ} can then be tuned to match that 1.8V reference with its known corresponding digital equivalent code of the DAC.

The size of M20 can be configured through a combination of switches. A first configuration technique, presented in Figure 5.8(a), consists in employing a transistor switch M20-2A in series with another transistor, M20-1A, whose gate is connected to M20 (i.e. V_{G20}). This technique divides the overall desired M20 size over several parallel switch-branches that can be independently enabled or disabled. Nevertheless, since M20-2A is in its triode region (i.e. having a small drain resistance), this technique is hard to adjust properly.

A second approach, presented in Figure 5.8(b), is similar to the one proposed in [21] and uses minimum-size transmission gates (M20-3B and M20-4B) in parallel with a complementary minimum-size pull-up. Transistor M20-1B has an $M \times W_{MIN}$ size. When V_{ON} is set to a logic high, the transmission gate connects the gate of M20-1B to V_{G20}; conversely, when V_{ON} is set to a logic low, it shorts the gate of M20-1B to $V_{DD,}$ thus turning the path through M20-1B off and disabling M20-1B's contribution to I_{20}. This second approach is faster than the first approach, since M20-2B, M20-3B and M20-4B are minimum-size transistors, whereas the serial technique in Figure 5.8(a) employs a M20-2A transistor having a size comparable to M20-1A ($M \times W_{MIN}$).

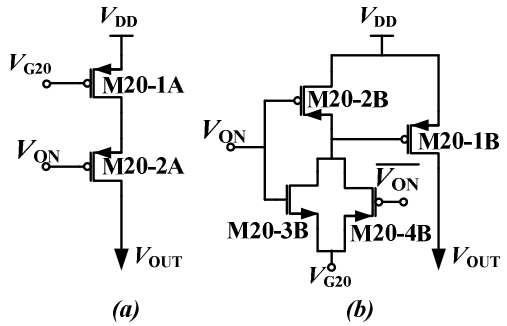

Figure 5.8 (a) Serial technique for changing M20 overall transistor size (Figure 5.7). (b) Parallel technique with transmission gate and pull-up used to change the overall transistor size.

5.3.8 A Fault Tolerant Network of ADCs and DACs

5.3.8.1 Proposed ADC-DAC architecture for a Unit-Cell

Any wafer-scale or large area integrated circuit (LAIC) must be defect tolerant to mitigate fabrication process defects. Because of the very large number of NanoPads (>1.2 M) and the fact that each pad must have access to both ADCs and DACs, a carefully planned architecture is proposed. The geometry of the WaferIC dictates that only two NanoPads with independent functionality can be operated at the same time within a Unit-Cell [3], [4]. Taking this into account, an architecture is proposed in which two ADC and DAC pairs are placed in parallel within each Unit-Cell. The ADC-DAC pairs are interconnected using a sharing network, such as to mitigate the impact of manufacturing defects in the WaferIC.

5.3.8.2 Proposed defect-tolerant resource sharing network

Unit-Cells are divided into two independent halves, each having one ADC, one DAC, serving eight NanoPads (see Figure 5.1 and Figure 5.9). Within a same Unit-Cell half, NanoPads may access either the ADC or DAC functionalities, but never both at the same time. The left half Unit-Cells share a common integrated metal and tri-state buffer grid, labeled GRID0. Likewise, the right-half Unit-Cells share GRID1 (see Figure 5.9).

Figure 5.10 shows how GRID0's integrated metal lines connect to the ADC and DAC within a Unit-Cell's left half using software-controlled tri-state analog multiplexers. An ADC's input may either arrive from its corresponding NanoPads, or from NanoPads that are located on the same

grid, either East or West of that Unit-Cell. Indeed, software-controlled transmission gates determine how signals between Unit-Cell halves on a same grid can propagate (see Figure 5.12). For example, if a uIC ball's signal needs to be sampled by any of the NanoPads on Figure 5.12, its corresponding analog buffer will propagate the signal to the nearest functioning ADC. This may either be the ADC corresponding to the NanoPads in contact with the uIC ball, or the first working ADC located either East or West on the same grid. Likewise, the DAC's output may either be sent through a tri-state analog buffer to the left-half Unit-Cell's NanoPads, or to a set of NanoPads located East or West on the same grid. Note that the DAC's generated signal is simultaneously output to all of the NanoPads on a same Unit-Cell half.

GRID0 and GRID1 each implement a defect-tolerant network (see Figure 5.9 and Figure 5.11), since they allow for NanoPad signals to skip faulty Unit-Cells and be routed to the closest functioning ADC or DAC. In its current form, due to silicon-area constraints, the defect-tolerant network was only extended horizontally (East to West), but in theory it could additionally be extended in the vertical direction (i.e. North to South).

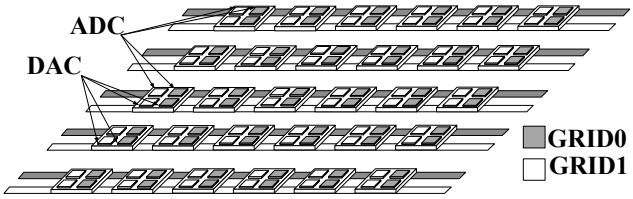

Figure 5.9 Proposed network for sharing ADCs and DACs over the full WaferIC.

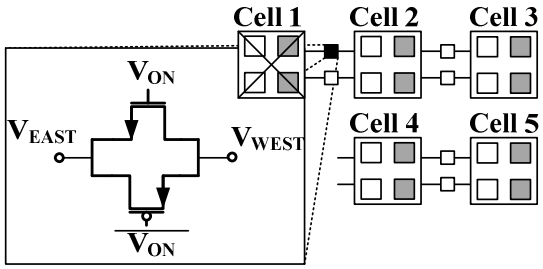

Figure 5.10 Transmission gate network allowing east/west analog signal propagation, given a faulty Unit-Cell 1.

Figure 5.10 shows a set of five Unit-Cells distributed onto two rows. In this example, the objective is to either sample or generate a signal on Cell 1's NanoPads. Nevertheless, Cell 1 is faulty. Under normal circumstances, the ADC or DAC within this Unit-Cell would accomplish

this task, but given that it is faulty, the proposed network allows for propagating the signal to its eastern neighbor's DAC or ADC through the use of a transmission gate. Using this technique, Cell 1 NanoPads will be able to employ the converters in Cell 2 to accomplish the task. Forwarding an analog signal requires an exclusive access of the grid segment between the faulty cell and the cell replacing its functionality, but it allows for the other Unit-Cells to remain otherwise untouched. Moreover, when forwarding analog signals, more than one faulty cell may be skipped. Indeed, the best-case scenario, for a reticle-image comprising an array of 32×32 Unit-Cells where every converter is operational, 32×2 ADCs or 32×2 DACs per row are available. As a consequence, NanoPads above a faulty Unit-Cells can be wired to any of the up to 31 available alternative ADCs or DACs on the same grid.

5.3.9 Results

5.3.9.1 Die of test chip and layout

The test chip, manufactured using a 0.18 µm CMOS technology, is shown in Figure 5.13. Each Unit-Cell is 560 µm ×560 µm in size and the NanoPads are 77 µm ×110 µm in size. The rest of the silicon area is employed for other digital components that are essential for the WaferIC, such as the JTAG chain for configuration. This buffer was design to be able to drive a capacitive load of 1 pF. The DAC's active silicon area measures 72.5 µm × 38.4 µm (0.00278 mm^2), which is roughly one third of a full-sized NanoPad. Within the DAC, the configurable unbalanced buffer accounts for 0.00132 mm^2, representing half of the active area, while the remainder is occupied by the BGR and the 1:1 analog buffer.

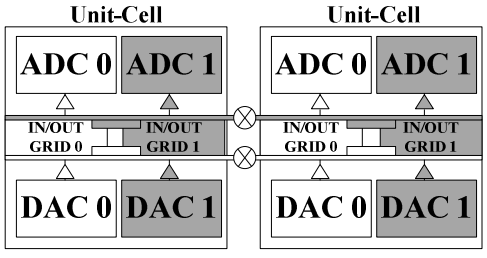

Figure 5.11 Unit-Cells are composed of two independent halves, each having one ADC and one DAC. Unit-Cell left-halves are connected to GRID0 and Unit-Cell right-halves are connected to GRID1.

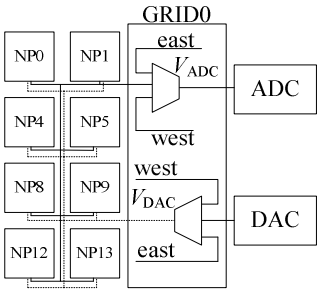

Figure 5.12 A Unit-Cell's left-half ADC input is either connected to its own NanoPads, or to NanoPads connected to GRID0 on a neighboring cell to the East or to the West of the given Unit-Cell. Likewise, its DAC output is connected to either its own NanoPads, or to NanoPads on a neighboring cell to the East or to the West on GRID0. Note that a Unit-Cell half either enables the ADC or the DAC (but not both at the same time)..

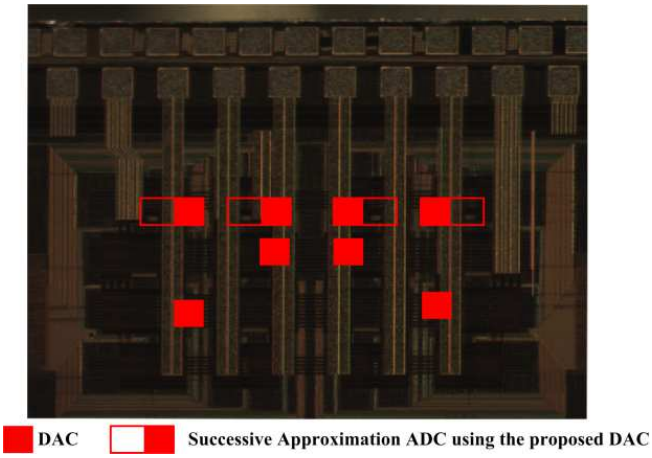

Figure 5.13 Die of test chip: two Unit-Cells are shown, comprising a total of 4 DACs and 4 SAR-ADCs.

The layout constraints of the WaferIC require that a certain silicon area within each NanoPad be reserved for the proper operation of other circuits, such as linear regulators and digital I/O. The proposed SAR-ADC and DAC are split and fit into two adjacent NanoPads to meet the silicon area constraints. Indeed, the SAR Digital Controller is separated from its other necessary components (DAC, Comparator, and the Sample/Hold circuits). The SAR-ADC's digital controller has a size of 72.5 µm×39.3 µm, and generates the 8-bit address for the DAC located on

its right (see Figure 5.14). The combined DAC, Comparator and Sample/Hold circuits have a total silicon area of 72.5 µm×39.6 µm, which is a very small when compared to the standalone DAC. Likewise, the other DAC (on the left) is also split into two : the DAC itself, and an 8-bit Serial-to-Parallel Converter used to address the DAC (see 0). The Serial-to-Parallel Converter is required to interface with the rest of the WaferIC, which is architected as a massive serial and digital interconnection network.

5.3.9.2 DAC characterization

The proposed DAC was validated experimentally for all 256 possible digital inputs values, and their corresponding output voltages, ranging from 864 mV up to 2.538 V, are shown in Figure 5.15. The DAC output is monotonic, with a LSB step that ranges from 100 µV to 24 mV and an average LSB of 5.6 mV. Figure 5.15 also shows that the predicted V_{OUT} from (8) and (10) follows the experimental results, and that M2 falls into the triode region around a digital input of 95 to 140 (as per Figure 5.6), for a corresponding output voltage ranging between 2.1 and 2.35 V.

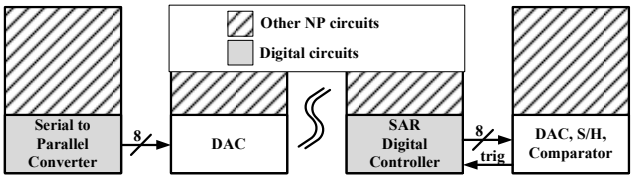

Figure 5.14 Layout floorplan of the proposed SAR-ADC and DAC network within a Unit-Cell

The Differential Nonlinearity (DNL) of the DAC, shown in Figure 5.16, was computed using the calculated LSB from (8) and (10). Normally the DNL is measure using a straight line. However, as mentioned before the proposed configurable analog buffer used as a DAC do not offer a linear output. Thus comparing its response with a straight line would not reflect the overall accuracy of the proposed DAC.

The measured DNL of the presented DAC has an overall average DNL of 0.41. A clear break can be observed at the digital input value of 113 : this is due to M20 (see Figure 5.7) entering its triode region, thus increasing the DNL. Below a digital input of 113, the average DNL is equal to 0.163, which is an improvement by a factor of 4. By using a scenario where several V_{IN} would have been used, thus M20 would never leaves the saturation region, as is described in

Section II.C, which would have greatly improved the DNL when the digital input value is over 113.

Notice that, as shown in Fig. 15, this proposed DAC is not linear, the INL measurement of only the DAC would not be representative and not fit for the requirement of the WaferIC and thus not presented. Be aware that, this proposed circuit is dedicated to propagates analog signals throughout the whole WaferIC. Our ADC samples the analog input signal using this proposed DAC with a successive approximation architecture. This digital signal is then propagated into a digital interconnection network and converted back to an analog signal at any other NanoPAds on the WaferIC with the same proposed DAC which suffers from the same non-linearity. Joint with a calibration method of the DAC, the same voltage level would be propagated through the WaferIC with respect of the precision of the proposed DAC.

Figure 5.18 depicts a sine wave that was generated by the proposed DAC, for which the operating frequency is 23.5 Hz and the peak-to-peak amplitude is 1.479 V. A look-up table based code converter was used to address the DAC, configured to compensate the DAC non-linearity shown in Figure 5.15. In order to apply a single DAC word configuration, the manufactured test chip requires 376 serially entered configuration bits. The serial mechanism that allows entering these bits in the test chip was successfully tested at a maximum frequency of 2.2 MHz. Due to test bench limitations of the test set-up, higher frequencies could not be test successfully. Moreover, the implemented DAC was designed to drive low integrated capacitive loads that are close to 1 pF. As a consequence, the settling time was approximated using two scope probes having different input capacitances (8 F and 12 pF). Indeed, by calculating the output capacitance of the DAC combined with the parasitics from the bonding of the package pins with the PCB trace, it was possible to estimate a more realistic output capacitance (see Tableau 5.2).

Several measurements were performed and are shown in Tableau 5.2, where an 8 pF and a 12 pF probe were used. From this table we can calculate that the capacitance associated with the parasitics and the DAC output has a value of 4 pF. According to the authors in [23], the package and the PCB parasitics can have a value of up to 8 pF. In [1] it is stated that a typical I/O pad, including the bonds, is typically around 5 pF. By calculation, we can assume that the parasitics from a PCB line have a value of around 3 pF. The settling time was thus computed by scaling the measured response time, using a 12 pF probe, to a 1 pF load (calculated as 4 pF minus 3 pF for

the PCB line). This is a conservative approximation, since the calculated results still include the parasitics associated with the package bonding. The computed settling time ranges from 62.5 ns for 1 LSB to 100 ns for the full-scale operation, which corresponds, roughly, to a 10 MS/s DAC. This approximation is close to the post-layout simulation results, which excluded the package parasitics, and where a settling time closer to 20 ns was obtained.

Figure 5.19 is the Fast Fourier Transform (FFT) extracted from the signal in Figure 5.18. The corresponding Spurious Free Dynamic Range (SFDR) has a value of 42.31 dB. Using these results, a Signal to Noise Ratio (SNR) of 51.97 dB, a Total Harmonic Distortion (THD) of 49.52 dB, and a Signal-to-Noise and Distortion Ratio (SINAD) or 47.5dB can be computed. The corresponding Effective Number Of Bits (ENOB) is thus calculated to be equal to 7.6 bits.

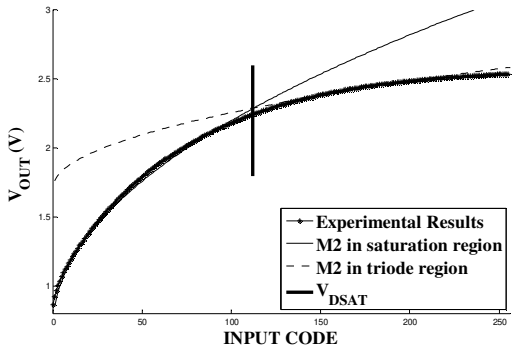

Figure 5.15 Measured V_{OUT} for all digital inputs to the DAC.

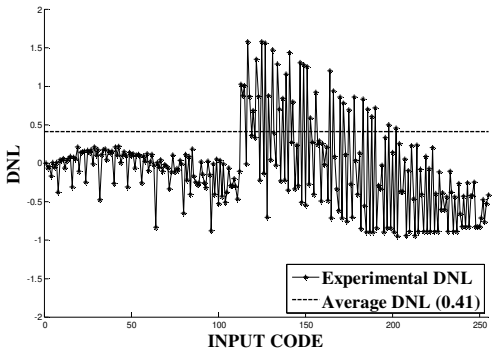

Figure 5.16 Measured DNL of the proposed DAC where the average DNL is 0.41

The SNR, the TDH, and the SINAD were calculated as per [22] using (14), (15) and (16), and data from Tableau 5.2.

The DAC calibration was performed using V_{ADJ} (Figure 5.7) to increase or decrease the biasing voltage, such as to slightly decrease or increase the output voltage of the DAC. In a circuit reuse idea as mention in the previous section this voltage is to be set by another DAC of the 300k present on the WaferIC acting as a reference voltage to set V_{ADJ}. The resulting output voltage variation of 25 mV is equivalent to about 4 LSB steps. Figure 5.17 shows that when operating between 1.5 and 2.2 V, V_{ADJ} can be used to obtain a ±12.5 mV linear displacement of the DAC output. Figure 5.17 also shows that the output voltage variations with respect to V_{ADJ} shows a good DC power supply rejection, thus, ensuring that the output range will vary by the same offset when adjusting V_{ADJ}.

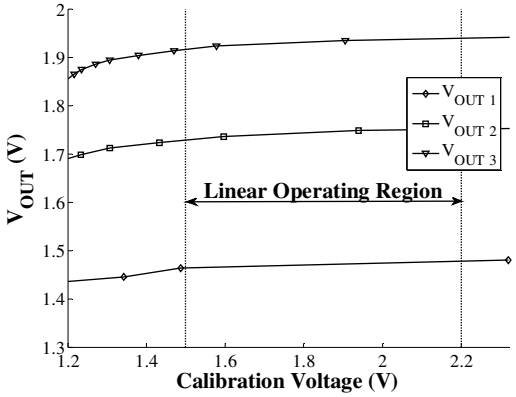

Figure 5.17 Calibration range using V_{ADJ} signal in order to precisely set the DAC voltage output.

5.3.9.3 Comparison with existing work

Table V. compares the work reported in this paper with recently published DAC architectures. In the context of wafer-scale integration, that is, to be able to integrate a network of over 150k DACs and 150k ADCs that can operate in parallel, the per-bit-size of the chosen design is a very important metric. The possibility of dynamically calibrating both DACs and ADCs is also vital, since process, voltage and temperature variations are large throughout a 200 mm wafer. The proposed architecture achieves a very small silicon area of less than 0.00035 mm^2/bit, which is almost 20 % smaller than the solution proposed in [23]. Furthermore, this is achieved without

sacrificing the overall performance since the average DNL obtained is comparable to competing designs with an ENOB of 7.6.

Tableau 5.2 Experimental results

Bit	Settling Time 12 pF (µs)	Settling Time 8 pF (µs)	Estimated Settling Time (ns)
MAX	1.6	1.2	100
Calculated V_{OUT} capacitance of 4 pF (16 pF total with probe)			
	Settling time 12 pF + 3pF+ 1pF (µs)		Estimated Settling Time 1pF(ns)
0 (LSB)	1.0		62.5
1	1.0		62.5
2	1.2		75.0
3	1.4		87.5
4	1.4		87.6
5	1.4		87.5
6	1.4		87.5
7 (MSB)	1.4		87.5
NOISE FLOOR: 58 dB		***fs*:10MS/s**	
Harmonic	Amplitude (dB)		
V1	-49.6		
V2	-50.8		
V3	-50.8		
V4	-52.4		

V5	-51.2
SNR: 51.97 dB **THD: 49.52 dB**	**SINAD: 47.50 dB** **ENOB: 7.6 bits**

$$\text{SNR} = \text{NOISE FLOOR} - 10\log_{10}\left(\frac{fs/2}{\text{BW}}\right) \quad (14)$$

$$\text{THD} = 20\log_{10}\sqrt{\left(10^{-V2/20}\right)^2 + \left(10^{-V3/20}\right)^2 + \ldots + \left(10^{-V5/20}\right)^2} \quad (15)$$

$$\text{SINAD} = 20\log_{10}\sqrt{\left(10^{-\text{SNR}/20}\right)^2 + \left(10^{-\text{THD}/20}\right)^2} \quad (16)$$

5.3.10 Conclusion

In this paper, a novel approach was proposed for designing ADCs and DACs that are intended for wafer-scale integration. The resulting system, which employs a novel and very compact DAC architecture, allows for over 150k DACs and 150k ADCs to be interconnected with a fault tolerant network. Indeed, the converter grids can share their analog output to mitigate the impact of any fault encountered in the network. The proposed DAC is based on an unbalancing technique that uses either a single or a multi-voltage reference to provide a wide selection of output voltages. Experimental results show that these DAC cover output voltage ranging between 864 mV and 2.538 V, with a resolution of 8 bits and a conversion speed of 10 MS/s. Moreover, an ENOB of 7.6 bits is achieved with an SNR of 51.97 dB and a SFDR of 42.31 dB. Finally, a dedicated dynamic calibration process allows for the DACs and ADCs to be fine-tuned to a range of 25 mV, thus allowing for any converter on the proposed network to be properly matched.

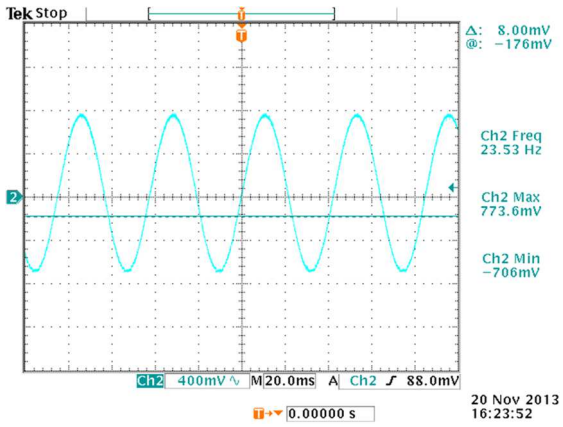

Figure 5.18 Generated sine wave based on 256 points using the proposed DAC

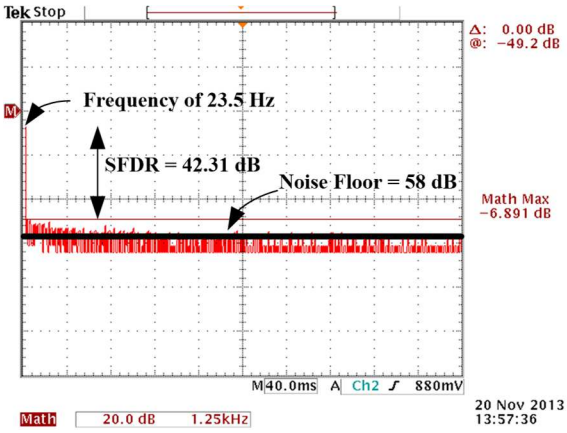

Figure 5.19 Associated FFT of the sine waveform generated in Figure 5.18 with 10k points.

Tableau 5.3 Comparison with existing works

	This Work	[26]	[43]	[44]
Technology	0.18 µm	0.13 µm	0.090 µm	0.18 µm
Year	2013	2016	2011	2012
Supply Voltage (V)	3.3	3.3	1.2/2.5	1.8
Resolution	8 bits	8 bits	12 bits	10 bits
DNL Average	0.41	N/A	<0.5	N/A

Speed	10MS/s	2MS/s	1.25GS/s	500 MS/s
Normalized Chip Size (mm^2)	0.00278	0.00099	3.3	0.034
Size Per Bit (mm_2)	0.00035	0.000012375	0.275	0.0034
ENOB	7.6	N/A	N/A	N/A
Calibration Process	YES	NO	YES	NO

CHAPITRE 6 DISCUSSION GÉNÉRALE

L'objectif principale de cette thèse de doctorat est d'améliorer le WaferIC et de l'élever à un niveau lui permettant d'accommoder n'importe quel circuit intégré. La version préliminaire décrite précédemment occupe la totalité de la surface de silicium disponible et ne supportant que les signaux numériques et ne disposant que d'un seul rail d'alimentation, ce qui entraîne des problématiques de dissipation de chaleur. Le plus grand défi a donc été de revoir la totalité de l'approche de la distribution de la puissance pour y libérer de l'espace et ensuite d'y inclure plusieurs autres fonctionnalités, tel que l'ajout d'un second rail d'alimentation ainsi que d'un réseau de CAN-CNA tolérant aux pannes permettant la transmission de signaux analogiques. Pour parvenir au résultat final, deux puces d'essai ont été fabriquées en technologie 0.18 µm, la première avec la TSMC et la seconde avec la fonderie TowerJazz.

Les résultats obtenus de ces deux puces d'essai ont permis l'écriture des quatre articles présentés dans cette thèse, en plus de valider l'architecture à savoir que toutes les fonctionnalités désirées utilisent la même surface de silicium que la version préliminaire. Il s'est même avéré que les efforts pour réduire la surface utilisée ont été si agressifs que la version présentée dans cette thèse nécessite une surface de silicium considérablement plus petite (~20 %).

CHAPITRE 7 CONCLUSION

Ce chapitre présente les conclusions générales ainsi que les contributions majeures de cette thèse de doctorat. Des suggestions et recommandations pour travaux futurs y sont également proposées.

7.1 Conclusions générales et contributions majeures

Dans cette thèse, trois articles ont été présentés et soumis ou publiés aux journaux suivants : publié à « *IEEE Transactions on Circuits and Systems I* », publié à « *Springer Science & Business Media Analog Integrated Circuits and Signal Processing* » et soumis à « *IEEE Transactions on Very Large Scale Integration* ».

La première puce d'essai a mené aux résultats qui ont été présentés dans le premier article qui fait l'objet du chapitre 3. Un régulateur linéaire à double rails d'alimentation de 1.8 et 3.3 V opérant de 500 mV jusqu'à 2.995 V en technologie CMOS 0.18 µm dans une surface de 0.008 mm^2 y est présenté. Ce régulateur linéaire peut fournir jusqu'à 40 mA avec un temps de réponse de 21.1 ns et une rejection du bruit de l'alimentation de 40 dB. Ce régulateur linéaire possède également en parallèle un plot d'E/S numérique configurable sur la même plage de valeur que le régulateur et pouvant atteindre une vitesse maximale de 250 MHz. La contribution majeure de cette puce d'essai ainsi que des publications en ayant découlées sont le partage de circuiteries ayant mené à une architecture plus compacte que ce qu'offre la littérature tout en conservant des performances s'y rapprochant.

Le second article présente une nouvelle topologie compacte d'un tampon analogique. Le circuit proposé utilise une paire différentielle modifiée et met à profit l'utilisation de deux étages complémentaires de type nMOS et pMOS afin de maximiser la plage dynamique de la tension de sortie. Le tampon proposé est également configurable quant à son courant de polarisation afin de pouvoir augmenter ses performances au besoin pour n'utiliser que le courant nécessaire pour y piloter la charge. Possédant un temps de réponse de 5.3 ns et opérant jusqu'à 194 MHz, il peut être configuré pour fournir un « *slew-rate* » entre 66 et 495 V/µs pour une surface de silicium totale de 0.001824 mm^2.

Le troisième article propose une nouvelle architecture de convertisseur numérique-analogique pouvant fournir une tension variant de 850 mV jusqu'à 2.538 V. Ce CNA possède une résolution de 8-bits et un nombre effectif de bit de 7.6 et un taux de conversion supérieur à 10MS/s dans une surface de silicium ultra compacte de 0.00035 mm^2. Ce CNA est intégré à un CAN par approximations successives et leur duo est étendu à un réseau tolérant aux défectuosités sur toute la surface du WaferIC. Plus de 300 k convertisseurs constituent ce réseau et permet la formation de bus analogiques pouvant propager des signaux analogiques d'un NanoPad à l'autre au travers tout le WaferIC. La contribution majeure de cet article est la réutilisation et le partages de circuiteries, dont la référence de tension configurable ainsi que le tampon analogique afin d'y assembler un réseau de CNA et de CAN tolérant aux défectuosités.

Un quatrième article en phase d'écriture et se retrouvant à l'annexe G, présente l'intégration de toutes les architectures présentées dans les 3 premiers et se veut une version miniature du WaferIC ou une matrice 7×8 Cellules y est présentée. Une extension du WaferIC vers la technologie des interposeurs 2.5D et 3D y est également proposée. Il a été démontré que l'architecture proposée peut fournir un courant jusqu'à 62 mA pour les deux rails d'alimentation pour une tension de sortie configurable de 850 mV jusqu'à 2.9 V avec un temps de réponse de 2.1 ns. Un plot numérique également configurable sur la même plage de valeur y est également présenté pour une vitesse maximale de 285 MHz. Le réseau de CAN-CNA tolérant aux pannes y est également présenté. La surface de silicium occupée est ~20 % plus compact que la version préliminaire du WaferIC et y présente beaucoup plus de fonctionnalités. La contribution majeure par rapport à la littérature est l'apport de circuiteries actives aux interposeurs. Ceux-ci sont typiquement passif et y intègre que des connexions métalliques ainsi que des composantes passives. L'extension du WaferIC aux interposeurs rendrait ceux-ci beaucoup plus versatile.

7.2 Recommandations pour travaux futurs

Cette section discute des recommandations pour travaux futurs ou des améliorations possibles des suites des travaux de recherches effectués dans le cadre de cette thèse de doctorat.

7.2.1 Distributions de la puissance

Afin d'améliorer la distribution de la puissance dans la structure proposée du WaferIC ou 1 régulateur linéaire asservi 8 NanoPads et de diminuer la résistance sérielle ajoutée par les longues

lignes de métal intégrées, un réarrangement des CPADs est suggéré. La disposition actuelle est une matrice 2×4 où tous les CPAD sont positionnés à une distance différente du régulateur. Un arrangement en étoile est proposé pour diminuer les longues lignes de métal et uniformiser la distribution de la puissance pour chaque NanoPad.

7.2.2 Calibration automatisée du réseau de CAN-CNA

La très grande taille du WaferIC, les variations du procédé de fabrication, la température et d'autres facteurs peuvent faire en sorte que deux convertisseurs identiques présentent des différences en performance et tension de sortie. De plus, vu le très grand nombre de convertisseurs, une calibration manuelle est exclue. L'automatisation de la calibration pourrait utiliser le rail d'alimentation de 1.8V comme tension de référence commune à tous le WaferIC (lorsqu'aucune puissance n'est requise) et inclure une circuiterie de comparaison de cette tension avec le 1.8V générée par le CNA.

7.2.3 Inclusion de tampon analogique dans le réseau de CAN-CNA

La résistance aux pannes du réseau de CAN-CNA proposé est basée sur la transmission d'un signal analogique vers une autre Cellule qui serait opérationnelle à l'aide d'une simple porte de transmission. Cela pourrait s'avérer problématique si la Cellule visée était trop éloignée ce qui entraînerait une dégradation du signal transmis. L'ajout ponctuel de tampon analogique permettant la transmission d'un signal analogique sur une plus longue distance pourrait être un ajout intéressant au réseau proposé.

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ANNEXE A – A Configurable Multi-Rail Power and I/O Pad Applied to Wafer-Scale Systems

A Configurable Multi-Rail Power and I/O Pad Applied to Wafer-Scale Systems

Nicolas Laflamme-Mayer, Yves Blaquière, *Member, IEEE*, Yvon Savaria, *Fellow, IEEE* and Mohamad Sawan, *Fellow, IEEE*

***Abstract*—We proposes in this paper a novel configurable multi-power-rail pad that combines power supply support circuits and a digital input/output (I/O) buffers designed for a wafer-scale system. This wafer-scale platform includes a reconfigurable wafer-scale circuit, the WaferIC, comprising an alignment-insensitive surface that can be configured to interconnect any digital components manually deposited on its surface. The proposed multi-power-rail pad minimizes power losses and heat dissipation within the circuit. The pad that is fed from two distinct voltage sources providing power at 1.8 and 3.3 V has been implemented and tested. This pad has two merged configurable control loops that can select the power source. Merging takes place through shared transistors. This dual supply pad embeds a voltage regulator that achieves a fast response time of 21.1 ns and that can operate over a wide range of configurable regulated output voltage, from 500 mV up to 2.955 V. This regulator is capable of providing a maximum output current of 40 mA while needing only a very small quiescent current of 126 µA. The regulator's power supply noise rejection ranges from -25 down to -40 dB for frequencies ranging from 1 kHz up to 1 MHz. The embedded digital I/O pad shares a common output with the power distribution and can be configured from 0.5 up to 3.3 V for a maximum speed of 250 MHz.**

***Index Terms*— Configurable, multi-power rail, I/O, LDO, NanoPad, Voltage regulator, WaferIC, Wafer-Scale.**

I. Introduction

Today's electronic systems are constantly growing in size and complexity. The increasing complexity combined with decreasing time to market makes it challenging for designers to meet cost and performance constraints.

A novel electronic system prototyping platform has been recently introduced to address these issues [1]–[3]. This platform is based on an active surface implemented using a 200 mm full wafer device. This active surface is covered with over 1.2 million tiny conductive pads called NanoPads interconnected with a configurable interconnection networks. Every Unit-Cell comprises a 4×4 array of NanoPads, and a 32×32 array of Unit-Cells defines a reticle image. The assembly at wafer-scale level is called WaferIC™ and is achieved by photo-repeating 76 copies of the reticle image that are stitched together to implement wafer scale interconnections [3].

When using the prototyping platform, user integrated circuits (uICs) are deposited on the active surface to build the target electronic system. This surface is designed to be insensitive to the alignment of deposited uICs (Fig. 1a). A thermal flexible pouch, filled with a thermal grease to evacuate heat, is put on top of the uICs firmly held in place by a uniformly applied pressure to ensure good electrical contact, with an anisotropic conductive film (Z-axis film) that embeds conductive vertical fibers (nickel needles) [4]. The Z-axis film also protects NanoPads from possible mechanical damage (Fig. 1b). A short-circuit detection mechanism maps all the uIC balls connected to more than one NanoPad, and the platform allows creating all the connections specified by a user netlist (Fig. 1c).

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The active surface must also feed power to the uICs. This is done from the bottom of the WaferIC using Through Silicon Vias (TSVs) for adequate signal integrity [3]. The top side of the WaferIC must be free of any other mechanical or electrical structures to ensure good electrical contact between uICs balls and the Z-axis film wires, which means that no decoupling capacitor or external components can be used on the WaferIC. The digital interconnection between two or more distant NanoPads is accomplished by the WaferNet™. This WaferNet is a very dense configurable interconnection network that spreads between Unit-Cells in every direction (N-S-E-W) with unidirectional connections of various lengths. These connections have lengths 2, 4, 8, 16 and 32, where for instance 8 means that the connected Unit-Cells are separated by 7 others [1].

The WaferIC needs to accommodate any type of uIC such as FPGAs, processors, SRAM and DDR memories resulting in a wide range of power supply requirements. For instance, a powerful processor (of size 40×40 mm^2) can requires 60 W [5] (an X86 device is used for reference) to correctly operate, causing intense heating if that power is fed to a 1.2 V device from a 3.3 V supply. In that case the theoretical efficiency would at best be 36%, with 165 W drawn from the power source, 60 W fed to the uIC, and 105 W lost due to joule heating in the embedded regulator. Thermal analysis shown that with adequate air flow and heat transfer the wafer can handle a maximum of 40 W of heat dissipation in the 40×40 mm^2 area occupied by the device package (for a 0.0016 mm^2 uIC), excluding the power absorbed by the uIC, for a total of 100 W or 62.5 mW/mm^2 [5]. This thermal constraint sets at 60 % the minimum required theoretical efficiency of the embedded regulator [3]. With that target efficiency, the embedded regulators should not use the 3.3 V supply to feed large amounts of power to the uIC at supply voltages below 2.0 V. This paper proposes a means to minimize thermal losses of distributed embedded linear regulators by feeding them from multiple power rails.

The following section describes the WaferIC and the constraints associated with its architectures. It also provides an overview of an existing solution for the embedded regulators for the NanoPads. Section III proposes a transistor level architecture for a configurable pad that can serve as an input, an output, or a power supply, and that can draw power from multiple power rails. The pad embeds a novel fast regulator that takes advantage of several power supply sources in order to improve power efficiency when providing power at low voltages as well as a configurable digital I/O. Section IV gives the experimental results measured from a testchip exploiting the proposed architecture that was implemented using the TSMC 0.18 µm CMOS technology. These results demonstrate the benefits of the proposed topology. Experimental results are detailed, discussed and compared with other published works.

II. WaferIC Description and Existing Solutions

A. The WaferIC

A structural view of two WaferIC's Unit-Cells is shown in Fig. 2, where 54 % (hatched area) of the silicon area is dedicated to digital circuits such as the WaferNet and the JTAG circuitries used to configure the WaferIC. The remaining 46 % area is for NanoPads. Each NanoPad can be configured as a ground, a power supply providing up to 3.3 V, a configurable digital output compatible with voltage supplies ranging from 0.5 V up to 3.3 V, a CMOS digital input or an open circuit (high impedance) [3]. The silicon area is one of the most important issues for the WaferIC closely followed by the quiescent current. Table I lists the foremost objectives and constraints regarding the WaferIC output capabilities and physical restraints.

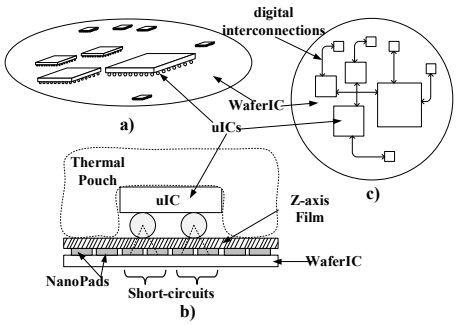


Fig. 1. (a) WaferIC with user integrated circuits (uICs) deposited on its alignment insensitive surface. (b) Platform cross-section where pressure in the thermal pouch ensures good electrical contact between uIC balls and the NanoPads through a Z-axis film. (c) Interconnection of uICs through the WaferNet.

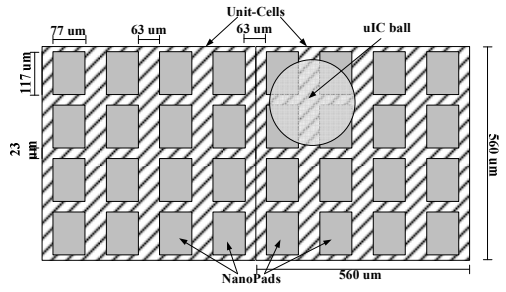


Fig. 2. Unit-Cell and NanoPad sizes where the hatched area is dedicated to digital circuits and WaferIC configuration and the grey area to the NanoPads.

Table I. Summary of the NanoPad (NP), Unit-Cell (UC), Reticle Image (RI) and WaferIC (WIC) voltage output capabilities and physical characteristics and requirements.

	Number	Max Current	Output levels	Area (mm^2)
NanoPad (NP)	16/UC	>50 mA	0.0 to 3.3 V	0.00847
Unit-Cell (UC)	1024/RI	>100 mA	-	0.3136
Reticle Image (RI)	76/WIC	5A	-	321.1264
WaferIC (WIC)	-	380 A	-	24405

The prototyping platform uses a hierarchical approach for power distribution: the first stage is a PCB that feeds 12 V to miniature PCBs (PowerBlocks). Each PowerBlock powers up to 4 reticle images made of 32×32 Unit-cells and converts this input voltage to 1.8 and 3.3 V. These voltage supplies provide power to the WaferIC through the TSVs. NanoPads act as the leaves of the system with access to 1.8 and 3.3 V power supply rails via massive integrated metal grids [3]. Notice that each NanoPad is ESD protected and transistor in the proposed regulator and protected from high voltage stress. To accommodate the uIC ball in contact with the NanoPads, the voltages on the power rails are adjusted to provide power to the uIC power pins with the proper voltage through one or several embedded regulators found within each Unit-Cell. These regulated voltages sources should ideally provide any output voltages between 0 V and 3.3 V for a maximal theoretical efficiency of 30 % up to 75 %, where the excess power is dissipated in the form of heat in the silicon structure.

Switching regulators can attain very high power efficiencies of up to 95%, which would result in a power saving over 35 W for the example depicted earlier (60 W processor) [6]. However, such regulators typically require external passive components making them very hard to integrate in limited silicon area (Table I). As a fully integrated solution is required for the WaferIC, the switching regulator approach is not possible.

For a given output voltage, the efficiency of linear regulator directly depends on its power supply voltage. Lowering the 3.3 V power rail can be a suitable solution to improve power efficiency, as long as the circuitry itself still operates adequately. However, a lower power supply voltage reduces the maximum regulated output voltage. Moreover, the power distribution structure described in [3] offers limited possibilities to adjust the source supply voltage, since the power rails supply several thousand NanoPads, connected to different uICs with possibly different power supply requirements. In [3], the whole WaferIC is powered by 1.8 V and 3.3 V rails. The 1.8 V rail is dedicated to the cell logic core (WaferNet and JTAG), and the 3.3 V rail supplies power to all other analog circuits (e.g. NanoPads). Several reticle images (up to 4) are externally fed by a same voltage source. Considering the multiple simultaneous requirements, lowering the supply voltages to increase efficiency is not an option, since many other analog circuits or NanoPads obtaining their voltage power from a same electrical node need the full scale voltage of the power rail to operate correctly.

B. Single Rail Configurable Power I/O PAD

The design proposed in [3] takes advantage of a hierarchical topology derived from [7] in order to minimize quiescent current and silicon area consumption by sharing the maximum number of common circuitries. A master-slave topology is used in every Unit-Cell. In reference to Fig. 3(a), the top module uses a reference voltage (V_{SET}) shared between 16 NanoPads. The Fast Load Regulator (FLR) embedded in each NanoPad (Fig. 3b) uses V_{SET} to set the output voltage within the range of 1.0 V to 2.5 V. In addition, V_{SET} sets the digital I/O voltage levels. This technique leads to a reduction in silicon area by sharing the fast load regulator with the digital I/O to provide power through configurable voltage (V_{SET}), which avoids duplicating power stages for supplying the digital I/O. However, control circuits must be added to share this regulated power supply between the digital I/O and the load. This comes at the cost of speed for both the I/O and the FLR response time, since the pass transistor loads the digital output (large transistor) and a significant parasitic capacitance is added by its gate.

The configurable I/O pad proposed in [3] (Fig. 3) integrates a digital I/O within the regulation loop coupled with a boost technique using a differential pair. This digital I/O can be configured to fit standard CMOS voltages of 1.0, 1.2, 1.5, 1.8, 2.0, 2.5 and 3.3 V with a post-layout simulated bandwidth of over 300 MHz with a 5 pF load. This approach allows very high current capabilities within a unit cell that could supply more than 100 mA per NanoPad, with a theoretical 1.6 A maximum per Unit-Cell (16 FLR according to Fig. 3), with adequate integrated power distribution. That amount of power fed by the linear regulator over a 560 µm×560 µm Unit-Cell, implies considerable heat dissipation through the wafer. This is due to the fact that the maximum power efficiency of a linear regulator is $(V_{OUT})^2/(V_{DD})^2$. This fact limits the one rail approach in terms of the maximum output power that every NanoPad can provide within a small silicon area (such as a Unit-Cell).

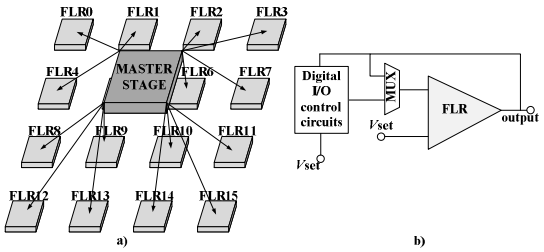


Fig. 3. (a) The master-slave topology proposed in [3] where a master stage feeds to 16 fast load regulators (FLR) a common reference voltage. (b) The embedded digital I/O proposed in [3] where the feedback signal is either controlled by the FLR or the digital I/O control circuits.

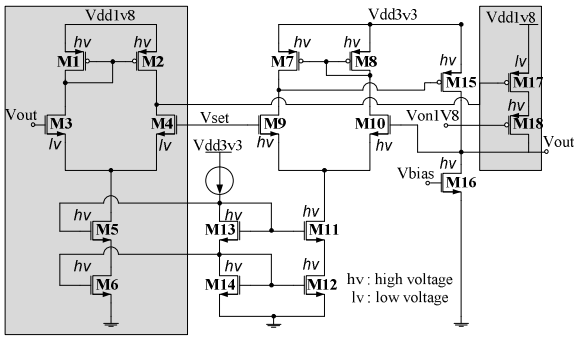


Fig. 4. Previous version of a dual rail regulator with separate feedback loops [10].

C. A Multi-Rail Power Supply for Power Efficiency Improvement

To maximize efficiency of the embedded FLR a multi-power supply rail was proposed in [8], where a multilevel converter using a single power supply rail is used to generate several output voltage levels using a multiplexed voltage supply or stacked voltage cells (independent cells put in series where the output voltage is a combination of them). This multi-rail approach can increase the power efficiency by 49 %. This efficiency depends on the source power supply and output voltage, with a maximum of 50 W of instantaneous power. Unfortunately this approach uses discrete components that make it incompatible with our embedded FLRs, where a fully integrated solution is required.

One of the drawbacks of such multiplexed approach is that it requires different power supply rails. The WaferIC is supplied from the bottom of the wafer using TSVs [3]. Studies in [9] show that the number of TSVs must be selected based on a trade-off between IR drops within the power grid and the mechanical aspects of the wafer itself. Having more vias makes the wafer more fragile. It was found that TSVs density must be limited to 0.25 TSV/mm^2 with our technology [9], which makes the addition of more power rails (as suggested in [8]) impossible.

A second drawback of the solution proposed in [8] is the maximum power it can supply in a sustained way. Each NanoPad has to push several milliamps (50 mA) to meet the WaferIC requirements listed in Table I. The proposed stacked voltage approach requires charge-pumps, which would introduce a lot of noise in the supplied power and ultimately limit the maximum current capabilities that can be obtained from the available silicon area.

D. A Configurable Power I/O PAD with Multi Power Rail Fast Load Regulator

To overcome the constraints on power distribution, silicon area, quiescent current and minimum required efficiency, a multi-power rail FLR is proposed. A preliminary version was proposed in [10] (Fig. 4) where a FLR uses dual 1.8 and 3.3 V rails with an overall improvement of 40% of the power efficiency when operating at low voltage (1.0 V) compared to the solution with only a single 3.3 V rail [10]. A drawback of this multi-power rail FLR is the duplication of all control circuitries used to assert the FLR, which is costly in terms of silicon area. Another drawback is that this architecture is optimized to operate at low voltages (such as 1.0 V) where 80 % of the current is provided by the 1.8 V rail [10]. This contribution from the lowest voltage rail to the output current drastically decreases as the output voltage gets close to 1.5 V, where the 3.3 V rail supplies most of the power. Notice that no mechanism is provided in this circuit to limit the current from the power supplies. A complementary solution is proposed in this presented paper where a single rail can be selected to minimize heat dissipation and silicon area.

With the solution proposed in Fig. 5 and Fig. 6, a silicon area similar to that reserved for the power transistors in the solution proposed in [3] will be used, where power rails are scaled down to handle only half the maximum current capability of the solution in [3]. This architecture benefits from a configurable control loop, power supply and bulk biasing. The principle is that when lower output voltages are required at the NanoPad, the 1.8 V rail is activated for a maximum theoretical efficiency from 55 % up to 83 % (1.0 and 1.5 V output voltages).

A challenge with multi power rail systems is the potential for latch-up. To prevent any possibilities of latch-up, protection transistors (switches) were added. With these transistors, it is possible to ensure that only one power rail at a time is tapped. Specifically, transistor M14 (Fig. 6) must be turned off when V_{OUT} (drain of M14) is larger than the branch power supply V_{DDn}. M14 is turned off using the voltage V_{BASE} that provides static bulk biasing for M13 and M14 and that also feed the control loop with the suitable supply voltage. When the V_{DDn} rail is in operation, M13-M14 bulks (V_{BASE}) are set to V_{DDn}. When not in operation the

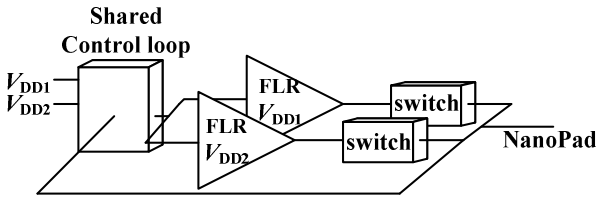


Fig. 5. Multi-power rail FLR sharing a common configurable control loop.

bulks are biased at the highest voltage, V_{DD1}. Table II summarizes key characteristics of a previously reported solution and of the proposed solution for a configurable power I/O pad suitable for the WaferIC described in this section. It shows that for the same silicon area the proposed solution offers an extended output range, better power efficiency, and comparable I/O speed but at the cost of a smaller maximum output current per rail (50 mA instead 110 mA). However, the same power is still available throughout the whole WaferIC.

III. Multi-Power-Rail Regulator Architecture and Circuit Implementation

This section details the circuit implementation for the proposed the multi-power-rail voltage regulator and I/O. It corresponds to a fabricated dual power rail, which can be extended to a multi-power rail configuration. The proposed architecture combines two separate fast load regulators operating with two power supplies (1.8 and 3.3 V). It is possible to operate one FLR at a time while sharing the same voltage feedback loop. Switches and dynamic bulk biasing are also added to prevent latch-up and ensure a good isolation of the non-operating FLR. The total current budget can be divided by the number of implemented power rails. In our particular case, a 110 mA total possible current is divided over 2 power rails occupying the same silicon area. This multi-power-rail regulator uses one common voltage reference generated in each Unit-Cell by a configurable bandgap in the master stage (Fig. 3) as in [3]. This bandgap based voltage reference nominally produce the same voltage throughout the entire silicon wafer, in order to produce a steady operating voltage on V_{OUT} when the temperature

Table II. Comparison of previously reported and proposed solution of power I/O pad for a single or multi-power-rail.

	Previous Solution [3]	New solution
Active Silicon Area	110 µm×77 µm	110 µm×77 µm
Power Supply	3.3 V	1.8 and 3.3 V
Maximum output current	110 mA	50 mA (each rail)
Power efficiency @ 1.0 V	~30 %	~55 %
Power efficiency @ 1.5 V	~45 %	~83 %
Possible regulated output voltages	1.0 to 2.5 V	0.5 to 2.995 V

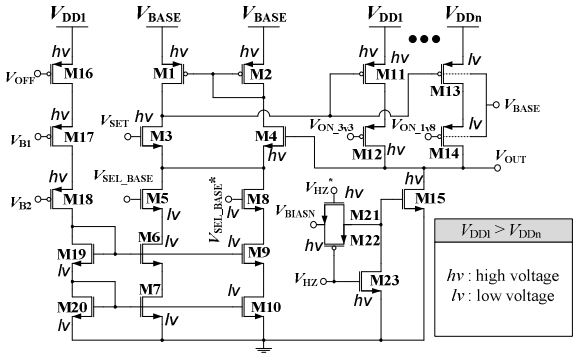


Fig. 6. Transistor level of the proposed configurable multi-power rails FLR with 1.8 and 3.3 V power rails.

increases or when there are slow variations (<kHz) in the power supplies.

A. Multi-Rail Voltage Regulator Circuits

The proposed multi-rail voltage regulator combines several separated feedback loops into one (two in the presented paper). According to the desired output voltage, determined by V_{SET}, (Fig. 6), the regulator can be configured to use either one of the two implemented supply rails, which are designed to operate at 1.8 V and 3.3 V, in order to limit the energy dissipated into the WaferIC. A main objective of combining both loops is to share circuits as much as possible. As listed in Table I, the useable active silicon area of a NanoPad is 0.00847 mm^2 for a 0.18 µm CMOS technology implementation. Sharing the large transistors found in the control loop, such as M1 to M4 and M7 to M10 (Fig. 4) results in savings of a 45×20 µm^2 per rail, which represents 11 % of the total available silicon area for a NanoPad. With the proposed circuit implementation, adding a power rail marginally increases the silicon area since few small size transistors (such as M5 to M7) are added, as well as another one for V_{BASE} selection.

The whole configurable feedback loop shown in Fig. 5 is made of transistors M1 to M10, where M1 and M2 form a simple current mirror, while M3 and M4 form a differential pair comparing V_{OUT} (the regulated output voltage shown in Fig. 6) and input V_{SET}. The output voltage V_{OUT} is fed back through M4 and the transistors in the branches V_{BASE} and GND are powered by V_{BASE}. The voltage V_{BASE} is connected to either 1.8 V or 3.3 V, according to the desired tapped power rail, using the digital signal V_{SEL_BASE} (Fig. 7). The biasing of the control loop is asserted by two independent and mutually exclusive branches formed by M5 to M7 when V_{BASE} = 3.3 V, and by M8 to M10 when V_{BASE} = 1.8 V (Fig. 6). The branch selection is controlled by the digital signals V_{SEL_BASE} and V_{SEL_BASE*}, its complement connected to M5 and M8 respectively. This design adequately biases the relevant differential pair according to the power rail connected to V_{BASE} to optimize the transient response and slew-rate of V_{OUT}.

A proper bulk biasing also has to be set according to the selected power rail to avoid latch-up. When V_{BASE} is connected to the 3.3 V rail, the bulk of M14 (low-voltage transistor) is set to V_{BASE} = 3.3 V. Indeed, if V_{BASE} was connected at 1.8 V direct biasing of the drain to substrate junction would occur and current would be fed to the substrate when V_{OUT} is larger than 1.8 V. Transistor M15 is biased with V_{BIASN} so that it always sinks a small current (hundreds of micro-amps) to activate the control loop and set V_{OUT} to the desired V_{SET}.

B. Quiescent Current Management

Reducing quiescent current of inactive modules to leakage levels is essential in the WaferIC. For example, in our application, a low quiescent current of 100 µA per NanoPad times 1.2 million of them in a 200 mm wafer would give a total static consumption over 100 A. A tenfold decrease in this quiescent current is possible but it would significantly degrade the slew-rate and transient response of the control loop and the FLR performance would degrade accordingly. Desirable as it is from a static consumption standpoint it is highly undesirable from a dynamic performance standpoint. A new approach is proposed here to allow a relatively high quiescent current in active NanoPads, while keeping the overall total current low.

To minimize static power dissipation, only NanoPads in contact with uIC's power pins are activated. These active NanoPads represent a small fraction of the NanoPads. A shut-down or sleep-mode approach is more amenable to bring the quiescent current of inactive NanoPads close to 0 A and therefore to control the overall static power consumption. When a NanoPad is in its OFF mode, the sinking current is in the magnitude of nanoamps, leaving a greater amount of available power for the active NanoPads (milliamps). For example, a Virtex 5 FPGA with a FF323 BGA package has 36 power pins, or 12 % of its relevant uIC pins [11]. When converting this into a NanoPad occupancy rate over the prototyping platform, this number decreases dramatically. For instance, a 40×40 mm^2 package covers an array of 71×71 Unit-Cells that comprise 80 656 NanoPads. If every pin of the package is in contact with 4 NanoPads it would result in an overall 1.6 % array occupancy for the 323 pins or 0.18 % for the power pins. Taking this into account, a turned ON FLR in the NanoPad could benefit from sufficient current headroom (milliamps) to perform its task. Thus, only a small fraction of the NanoPads would be drawing some biasing current, which allow improving the FLR performance by using larger quiescent current when needed.

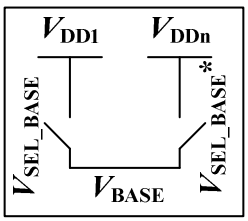


Fig. 7. Configurable power supply for the control loop and transistor biasing. Switches are made of large pMOS

The FLR sleep mode is activated first by cutting off the biasing branch of the control loop with the digital signal V_{OFF} and transistor M16 in Fig. 6. The remaining of the circuit power consumption is disabled by turning off both the output current path with V_{ON_1v8} and V_{ON_3v3} signals using M12 and M14 respectively. Another digital signal, V_{HZ}, has been added to prevent any current path to the ground through M15. Activating V_{HZ} puts the M15 transistor in its cut-off region by shorting its gate to GND with M23 and deactivating the transmission gate formed by M21 and M22, placing the whole multi-power rail FLR in a high impedance mode and thus drawing virtually only transistor leakage currents (nanoamps).

C. Configurable Digital Input/Output NanoPad

As stated in the introduction, when a NanoPad is configured as an I/O rather than a power supply, to support CMOS I/O signaling, it has to accommodate wide range of standard I/O voltages from 0.9 V to 3.3 V according to the uIC balls in contact with it. The use of I/O banks such as the ones found in FPGAs [11] is not a suitable solution for the WaferIC. It would require at least one voltage reference per Unit-Cell adding, an extra 77 824 TSVs. Another approach has to be used to fulfill the voltage configurability of the I/O. Most configurable I/O, like the ones in FPGAs, offer a wide range of I/O output drive such as 2, 4, 6, 8, 12, 16 and 24 mA [11] to accommodate different loads, fanouts, or PCB lines length. However, since a uIC ball is always directly connected to a NanoPad (direct connection), only the current sank by the load should be considered.

As mentioned in section III a, this paper proposes a small size multi-power rail FLR, combined with a multi-power rail I/O embedded in a configurable NanoPad interface circuitry. The reported implementation has two power rails (see Fig. 8). Previous work in [3] proposed a combined version where the digital I/O uses the main FLR as its configurable power source. However this method requires additional control transistors and adds a significant parasitic capacitance load on the gate of the pass transistor (transistor that supplies power), making the response time of the FLR slower. By separating these two functionalities, the response time of the main FLR does not suffer from this added capacitance.

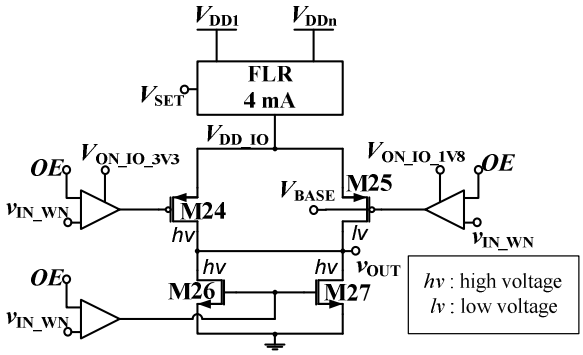


Fig. 8. Proposed configurable dual rail digital I/O 4 mA output drive.

The proposed I/O circuit has its output (v_{OUT}) connected with the 40 mA-FLR (the one with high current capabilities in Fig. 6) used for load regulation. The output voltage produced by the FLR ranges from 0.5 to 3.3 V, defined or set with the configurable signal V_{SET}, which is generated by a configurable bandgap reference (not discussed in this paper). The I/O was designed to offer a maximum current drive of 4 mA to fit the silicon area constraints. As shown in Fig. 8, the power fed by the 4 mA-FLR (V_{DD_IO}) supplies the I/O made of transistors M24 and M26 for the high voltage rail (3.3 V) and transistors M25 and M27 for the low voltage rail (1.8 V). Buffers drive the gates of each transistor with control signals $V_{ON\_IO\_3V3}$ and $V_{ON\_IO\_1V8}$ to ensure that only one path is active at a time. The output can also be placed in a high impedance state with the control signal *OE*. The signal v_{IN_WN} is a digital data signal coming from the WaferNet and propagating to the NanoPad output v_{OUT}. These buffers allow the low drive capability of the signal v_{IN_WN} to drive larger transistors such as M24 to M27. The identical high voltage transistor M26 and M27 have two functions: save silicon area and extend lifetime of M27. Effectively, having a single ground (digital level '0') for all configurable V_{DD_IO} allows a reduction of the needed silicon area at the cost of I/O speed when operating at lower voltage such as 1.0 V. However, using low-voltage transistor at M27 would have degraded its lifetime when v_{OUT} >1.8 V. The NanoPad digital input operation is done by a digital CMOS buffer (not shown). This buffer receives any digital input signal with V_{HIGH} between 0.9 V and 3.3 V, and it scales up or down the input voltage to a clean 1.8 V digital CMOS signal.

IV. Implementation and Experimental Results

To validate the proposed solution a test chip was designed and fabricated using TSMC 0.18 µm 6 metal layers CMOS technology. A microphotograph shows the actual fabricated chip (Fig. 9). The circuits includes a complete configurable dual rail FLR with power

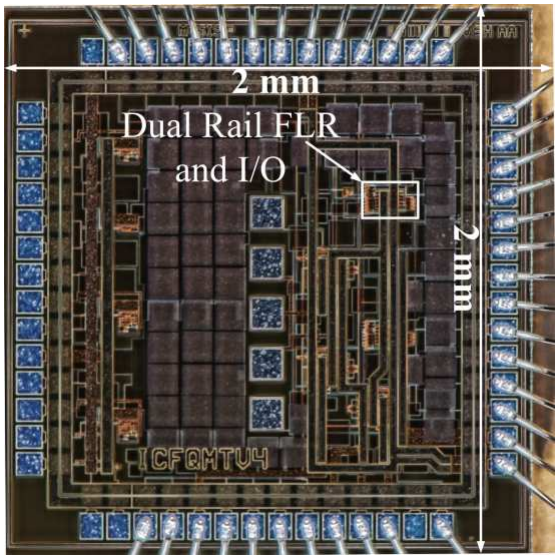


Fig. 9. Microphotograph of the fabricated testchip of the proposed multi-power rail power pad and I/O in a 0.18 µm technology.

supplies of 1.8 and 3.3 V, a configurable dual rail digital I/O, and a configurable bandgap that can produce and output value ranging from 0.9 up to 2.8 V for setting V_{SET} and others test circuits. The active area occupied by the FLR and the I/O is 100×80 µm for a total area of 0.0080 mm^2. The following section presents the experimental results regarding the main FLR, the maximum DC current for both rails for a wide range of output voltages, the regulation characteristics with an active load and the power supply noise rejection. Experimental results are also detailed for the embedded dual rails digital I/O.

A. DC Characterization

In the implemented design, the two power rails were not identically sized to provide the same amount of current. Indeed in most designs, uIC I/Os are powered-up at voltages higher than the uIC cores and more current is required by uICs cores (operating at the lowest voltages), thus the 1.8 V power rail was designed to have a current rating larger than the 3.3 V power rail. Fig. 10 and Fig. 11 show the DC characterization of the FLR for the 1.8 V and 3.3 V rails respectively. When the FLR is configured to use the 1.8 V rail, it can provide up to 60 mA with an output voltage as low as 500 mV using a single power supply. The average DC resistance for both rails is close to 4 Ω. The WaferIC structure forces a uIC pin to be in contact with a minimum of 2 NanoPads. A Virtex 5 FPGA with a FF323 BGA package has uIC balls of 500 µm of diameter [11]. In this case a single supplied ball would most certainly be in contact with around 10 NanoPads according to their geometries and sizes, which drops the overall DC resistance to 400 mΩ by having 10 FLRs working in parallel.

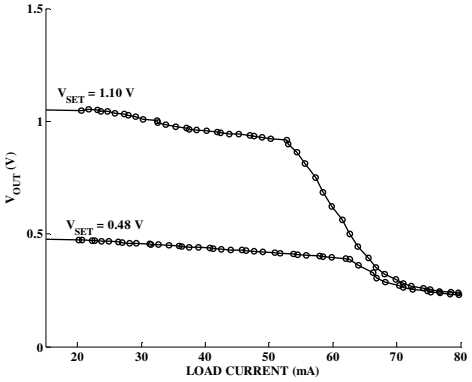


Fig. 10. DC characterization of the 1.8 V power rail low-dropout regulator

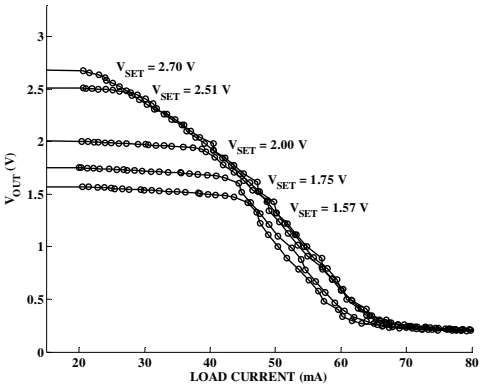
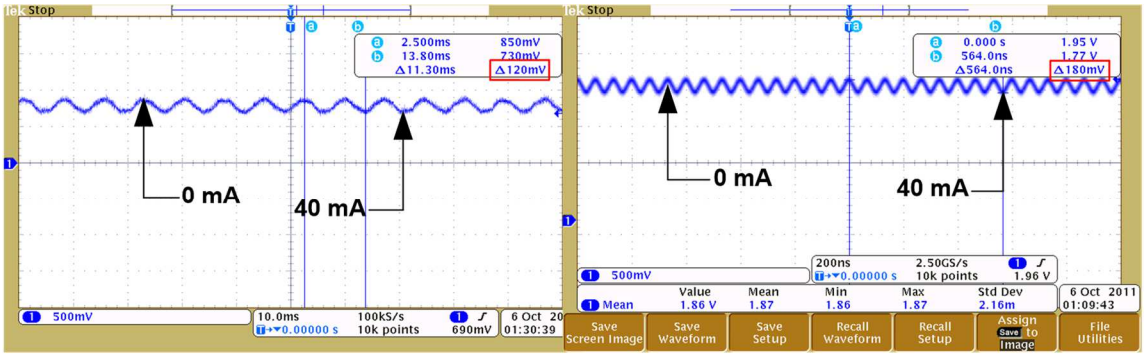


Fig. 11. DC characterization of the 3.3 V power rail low-dropout regulator

B. Response to an Active Current Load

According to the author in [12], the core capacitance of the power grid of a digital circuit in a 0.13 µm CMOS technology with a silicon area of 35 mm^2 has a typical value ranging from 14 to 30 nF. Smaller circuits can show smaller core capacitance down to ~2 nF. Our measurements were done with an equivalent core capacitance load of 4.7 nF, depicting an average size digital circuit, in parallel with an active current load that switches from 0 to 40 mA every cycle, with a 50 % duty-cycle. Transient characterization was performed at 3 different operating frequencies: 150 Hz, 1 MHz and 15 MHz for both power rails. A current output load of 40 mA with a 4.7 nF capacitance was used for all experiments, except when V_{OUT} is set to 2.60 V where the capability of the 3.3 V rail is not sufficient (according to Fig. 11). In this case, a 0 to 25 mA load was applied.

Fig. 12 (a) and (b) show a measured regulated V_{OUT} = 0.85 V and 2.0 V when the FLR is powered by the 1.8 V and the 3.3 V rails respectively. Table III summarizes the performance results. We observe that both power rails offer similar performance regarding the output voltage deviation (ΔV_{OUT}) and dynamic output impedance ($\Delta V_{OUT}/\Delta i_{OUT}$). They respectively range from 120 mV up to 200 mV and 3.0 Ω up to 6.6 Ω. The WaferIC would most certainly have several NanoPads in contact with a load (uIC ball), which would reduce the dynamic output impedance according to the number of FLRs working in parallel, boosting in proportion the performance reported in Table III.



a) b)

Fig. 12. Transient v_{OUT} response (Fig. 6) to a 0 to 40 mA current load with a 4.7 nF output capacitance (a) when supplied with the 1.8 V power rail for 150 Hz at V_{OUT} = 0.85 V. (b) when supplied with the 3.3 V power rail to a load of 40 for 15 MHz at V_{OUT} = 2.0V.

Table III. Performance summary of both power rail FLR with a dynamic load.

1.8 V power rail						
V_{OUT} (V)	0.850		0.900		1.50	
Current (ma)	40		40		40	
ΔV_{OUT} (mV)	150Hz	120	150Hz	160	150Hz	160
	1MHz	160	1MHz	160	1MHz	160
	15MHz	160	15MHz	160	15MHz	160
Dynamic output impedance (Ω)	3.0 to 4.0		4.0		4.0	
3.3 V power rail						
V_{OUT} (V)	1.50		1.80		2.60	
Current (mA)	40		40		30	
ΔV_{OUT} (mV)	150Hz	180	150Hz	160	150Hz	160
	1MHz	200	1MHz	200	1MHz	200
	15MHz	180	15MHz	180	15MHz	180
Dynamic output impedance (Ω)	4.5 to 5.0		4.0 to 5.0		5.3 to 6.6	

C. *Output Regulated Voltage Swing Capabilities and Quiescent Current*

The proposed multi-power-rail regulator must be able to accommodate any uIC deposited on its active surface in terms of power distribution, meaning that the regulated voltages should support a wide range of V_{DD}. Fig. 13 demonstrates the output capabilities of the proposed architecture in relation with the applied V_{SET}. The measurement clearly shows a linear relation between V_{SET} and V_{OUT} with a small DC offset less than 100 mV. The proposed system saturates at ~3.0 V in terms of regulated output voltage.

Each unused FLR can be turned off for minimum power consumption. By doing so, the leakage current drops to ~120 nA drawn on the 3.3 V power rail and as little as 25 nA on the 1.8 V rail. This low current consumption allows the proposed architecture to be integrated into a full wafer device. The overall maximum leakage current is 155 mA on the 3.3 V rail and only 31 mA on the 1.8 V rail.

D. *Digital I/O Characterization*

The proposed design implemented in the test chip also includes the embedded configurable digital I/O, described in Fig. 8, which shares the output (v_{OUT}) with the FLR. A high impedance configuration mode is a necessity for both structures to ensure that the regulation and I/O do not interfere with each other. The high voltage level produced by the digital I/O can range from 0.5 up to 3.3 V. Measurements shown in Fig. 14 were obtained when the configurable I/O is configured to produce output voltages of 0.5, 1.0 and 1.5 V using the 1.8 V power rail. We notice that the operating frequency depicted in Fig. 14 is 250 kHz. This low frequency is related to the test bench. Since both regulation and

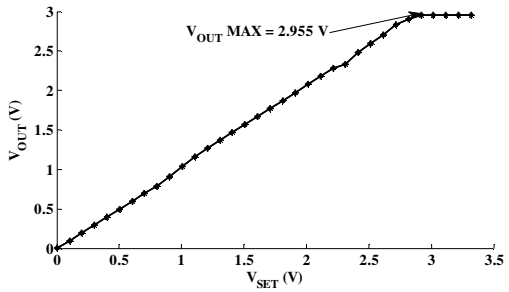


Fig. 13. Relation between the output voltage (V_{OUT}) and the configured voltage V_{SET}, of the proposed multi-power rails voltage regulator.

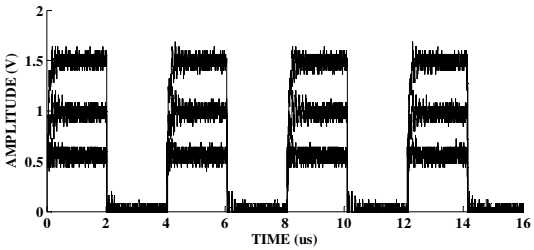


Fig. 14. Measured output voltage of the configurable digital I/O configured to provide 0.5, 1.0 and 1.5 V CMOS output voltages for a 250 kHz input signal.

digital I/O functionalities physically share the same output on the testchip, and the test environment was optimized for power delivery test, the maximum operating frequency is dramatically reduced due to all the extra parasitic capacitances introduced (~50 pF). Post-layout simulations including all parasitic capacitances and inductances were performed using Cadence and Calibre tools. It was found that the maximum operating frequency of the digital I/O is 250 MHz when the actual current drive of 4.2 mA is applied to a 5 pF load, which represents the typical capacitance of a uIC pin and bounding wire for a digital I/O [12].

E. *Power Supply Rejection Ratio*

Both power rails need to be insensitive to fluctuations on their own respective power supplies. Measurements were performed on both rails by injecting a sinusoidal signal superposed to a DC voltage of 1.8 or 3.3 V and by observing the output v_{OUT}. Fig. 15a shows V_{OUT} = 1.0 V with noise injection on the power supply corresponding to $V_{DD} = 1.8\ V_{DC} + 1\ V_{pp}$. At 1 kHz, we observe virtually no disturbance in the output voltage with more than -40 dB of noise rejection for this frequency on the 1.8 V power rail. The same measurements were performed at 10 kHz and 1 MHz with a slight change of stimulus ($V_{DD} = 1.8V_{DC} + 0.8V_{pp}$). The decrease of the sinusoidal input amplitude to 0.8 V in only due to equipment limitations at this frequency Again measurements show a noise rejection of more than -40 dB at 1 MHz. Table IV list the power supply rejection ratio (PSRR) of both rails.

Fig. 15b depicts a similar scenario but with a V_{OUT} = 2.5 V using the 3.3 V rail where V_{DD} =3.3 V_{DC} + 1 V_{pp}. Measurement shows similar noise rejection at lower frequency (1 kHz) between both rail, around -40 dB of noise rejection. A slight increase of the output noise occurs at 10 kHz where the noise rejection reaches -30 dB and -25 dB at 1 MHz.

Table IV. Performance summary of both power rail PSRR

1.8 V power rail		
V_{OUT} (V)	0.9 and 1.0	
V_{DD} (V)	1.8 V_{DC} + (1.0V_{pp}/0.8 V_{pp})	
PSRR (dB)	1kHz	-40
	10kHz	-40
	1MHz	-42
3.3 V power rail		
V_{OUT} (V)	2.0 and 2.5	
V_{DD} (V)	3.3 V_{DC} + (1.0V_{pp}/0.8 V_{pp})	
PSRR (dB)	1kHz	-40
	10kHz	-30
	1MHz	-25

F. Comparison with Existing Works

The proposed multi-power rails voltage regulator does not require any on-chip decoupling capacitor. This design is meant to work only with the parasitics conveyed by a uIC ball and its power grid (~1 nH, ~4.7 nF). This multi rail regulator offers a unique and novel possibility to draw power either from the 1.8 V or 3.3 V line resulting in power saving up to 25 % compared to a single rail design (as proposed in [3]).

Equation (1) gives the response time T_R calculated from the load (C_{LOAD}) the maximum voltage deviation (ΔV_{OUT}) for the 1.8 V power rail at 0.9 V operating at 15 MHz and the maximum current the regulator can provide (I_{MAX}). The measured response time with our design parameters is 21.1 ns.

$$T_R = \frac{C_{LOAD} \cdot \Delta V_{OUT}}{I_{MAX}} = \frac{4.7\ \text{nF} \cdot 180\ \text{mV}}{40\ \text{mA}} = 21.1\ \text{ns} \quad (1)$$

For comparison of various FLR, the Figure of Merit (*FOM*) described in (2) is used, where I_Q is the quiescent current [7]. As shown in Table V, this work achieves the best *FOM* by a hundredfold as well as being the most compact architecture even with a digital I/O integrated within its structure.

$$FOM = T_R \frac{I_Q}{I_{MAX}} \cdot APB$$
$$\Rightarrow 21.1\ \text{ns} \cdot \frac{126\ \mu\text{A}}{40\ \text{mA}} \cdot 0.0002 = 0.0000133\ \text{ns} \quad (2)$$

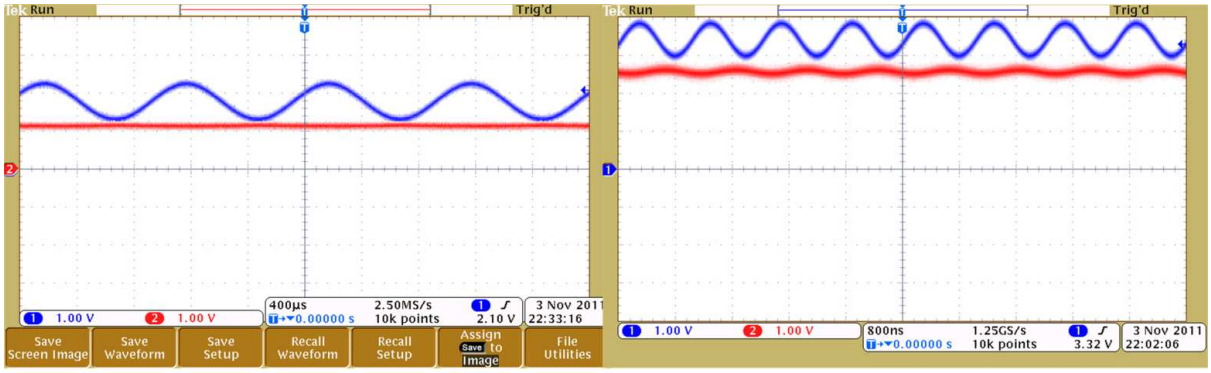
This work also achieves the widest regulated output range with almost 2.5 V, compare to 0.8 V for its closest competitor [13]. Moreover, this proposed architecture allows power saving when operating at lower voltages by using the adequate rail to minimize heat dissipation and greater power efficiency compared to its previous version. Power saving up to 25 % is achieved for V_{OUT} = 1.0 V and 30 % for a V_{OUT} = 1.2 V, while being more efficient in terms of silicon usage.

Table V. Performance comparison of the proposed FLR with different works

	[7]	[13]	[14]	**This Work**
Year	2005	2010	2012	2014
CMOS Process (µm)	0.09	0.18	0.065	0.18
Area (mm^2)	0.098	0.006	1.0908	0.0080
V_{IN} (V)	1.2	1.8	1.1	1.8 or 3.3
V_{OUT} (V)	0.9	0.9 to 1.7	0.5 to 1.0	0.5 to2.955
I_{MAX} (mA)	100	20	100	40
I_Q (µA)	6000	1.06	164.5	0.000145
Response Time T_R (µs)	0.00054	0.0015	0.0054	0.02115
Decoupling capacitor (µF)	0.00060	0.0005	0.0045	0.0047
FOM (ns)	0.0000314	0.0000632	0.0000969	0.0000133
Area per mA	0.00098	0.0003	0.010908	0.0002

V. CONCLUSION

A platform for rapidly prototyping electronic systems, the WaferBoard™, is being developed in our lab. It is based on a configurable wafer-scale active circuit. Electronic components firmly held in contact with its surface are powered and interconnected using circuits implemented in this active surface. This paper focuses on means for power delivery that mitigate heat dissipation by introducing a novel multi-power rail voltage regulator that operates from 1.8 V and 3.3 V rails. The addition of second power rail allows power savings up to 25 %, while offering a wider range of operation at the cost of reducing the total deliverable power per rail due to limitations in the available area. The proposed design merges two fast load regulators into one by using configurable power supplies, the bulk biasing technique and shared transistors. The proposed architecture was fabricated in a 0.18 µm CMOS technology and occupies a small area of 0.0080 mm^2 by combining the two control loops into one, which makes it suitable for wafer-scale integration. Moreover, the proposed design offers a fast response time of 21.1 ns, with a 40 mA load on either supply rail, and very low quiescent currents of 126 µA. This work also achieves the best Figure Of Merit that outperforms by a factor of 3 its closest competitors.



a) b)

Fig. 15. Output voltage v_{OUT} (red) when sinusoidal noise is injected on power rail (blue): (a) 1.8 V power rail with V_{OUT} = 1.0 V at 1 kHz. (b) 3.3 V power rail with V_{OUT} =2.5 V at 1 MHz.

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He has carried work in several areas related to microelectronic circuits and microsystems such as testing, verification, validation, clocking methods, defect and fault tolerance, effects of radiation on electronics, high-speed interconnects and circuit design techniques, CAD methods, reconfigurable computing and applications of microelectronics to telecommunications, aerospace, image processing, video processing, radar signal processing, and digital signal processing acceleration. He is currently involved in several projects that relate to aircraft embedded systems, green IT, wireless sensor network, virtual network, computational efficiency and application specific architecture design. He holds 16 patents, has published 97 journal papers and 354 conference papers, and he was the thesis advisor of 140 graduate students who completed their studies.

He was program co-chairman of ASAP'2006 and the general co-chair of ASAP'2007. He has been working as a consultant or was sponsored for carrying research by Bombardier, CNRC, Design Workshop, Dolphin, DREO, Genesis, Gennum, Hyperchip, ISR, LTRIM, Miranda, MiroTech, Nortel, Octasic, PMC-Sierra, Technocap, Thales,Tundra and VXP. He is a member of the Regroupement Stratégique en Microélectronique du Québec (RESMIQ), of the Ordre des Ingénieurs du Québec (OIQ), and was a member of CMC Microsystems board since 1999 and chairman of that board from 2008 to 2010. He was awarded in 2001 a Tier 1Canada Research Chair (www.chairs.gc.ca) on design and architectures of advanced microelectronic systems. He also received in 2006 a Synergy Award of the Natural Sciences and Engineering Research Council of Canada

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ANNEXE B – A Configurable Analog Buffer Dedicated to a Wafer-Scale Prototyping Platform

A Configurable Analog Buffer Dedicated to a Wafer-Scale Prototyping Platform

Abstract—**This paper concerns a novel configurable analog buffer dedicated to a wafer-scale prototyping platform of electronic systems. The proposed architecture uses complementary nMOS and pMOS stage buffers, which are built with modified conventional differential pairs used for maximizing the output voltage swing. This compact analog buffer offers several slew-rate features that range from 66 V/µs up to 495 V/µs with a quasi-unity gain and only uses 21 transistors for a total silicon area of 0.001824 mm^2. The bandwidth of this proposed buffer can be programmed from 74 MHz up to 194 MHz with response time up to 5.3 ns. This overall configurability allows better power management, reduces the power-supply noise injection within the wafer-scale platform, and diminishes the quiescent current.**

Index Terms—**analog buffer, wafer-scale, configurable, WaferIC, slew-rates**

I. Introduction

THE WaferBoard™ is a recently introduced wafer-scale prototyping platform of electronic systems [1]-[3]. This platform acts as a configurable support for user integrated circuits (uICs), where any type of signal or power can be fed to the uICs balls in contact with. This wafer-scale platform is populated with a sea of small conductive pads called NanoPads, which can be configured independently as a ground, a regulated voltage output, a digital input-output (I/O) or as an analog I/O. NanoPads are grouped in 4×4 arrays called Unit-Cells, and arrays of 32×32 Unit-Cells are called reticle-images (Fig. 1). Inter-reticle stitching build an assembly of 76 photo-repeated reticle-images into a 200 mm wafer-scale platform named WaferIC. The specifications of this chosen architecture were defined by previous work in order to obtain a maximum coverage of the wafer surface with NanoPads while leaving enough silicon room for the needed circuits. This prototyping platform was thus designed to support any uIC package with 250 µm ball diameter and 800 µm pitch [1].

Each NanoPad is a fully configurable power pad and I/O, which can deliver up to 110 mA with various

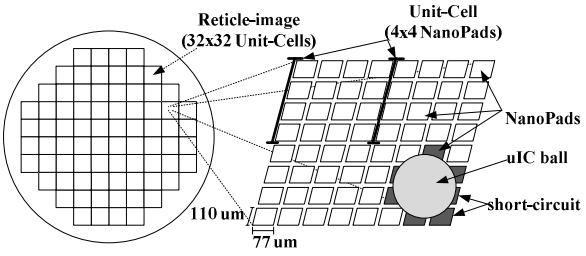

Fig. 1. Hierarchical view of the WaferIC™, the reticle-image the Unit-Cell and the NanoPad.

outputs voltage (0.9, 1.0, 1.2, 1.5, 1.8, 2.0, 2.5 and 3.3 V). When configured as an I/O, digital signals can propagate from a pad to any others within the WaferIC at a maximum frequency of 300 MHz and with the same output voltage as the power configuration defined previously (from 0.9 to 3.3 V) [3]. Signals communication between NanoPads is ensured by a dense fault tolerant network called WaferNet [4]. This network can send and receive signals in 4 directions (N, S, E, W) to/from neighbouring Unit-Cells using link of various lengths (1, 2, 4, 8, 16 and 32); where, for instance, a link of length 8 has 7 Unit-Cells between the two communicating Unit-Cells [4].

To propagate an analog signal between NanoPads within the WaferIC an analog to digital converter (ADC) and digital to analog converter (DAC) are needed. In this case a NanoPad samples the input analog signal and propagates it through the WaferNet as a digital signal. The receiving NanoPad converts back the original signal and outputs it. The conversion back to the analog world requires a buffer that can drive the load connected to it (the uIC ball) [5][6]. Analog output buffers are commonly designed to drive a large capacitive load, to minimize the static power consumption (quiescent current) and often rely on the use of operational amplifiers [7]. Other requirements such as the output voltage swing, rail-to-rail operation and the speed of the buffer are important criteria. Class-AB output buffer offers a good trade-off when low signal distortion, low quiescent current and good driving capabilities are the objectives. Other approaches found in the literature use push-pull [8], class-A [9] or class-B output buffer [10]. These approaches are limited in the overall speed

because they imply a high impedance output node with drain connected transistors only to drive the output [11]. Hence a dedicated fast operation buffer requires a low-output impedance having a source connected topology with a drain and gate connected together is more amenable [11].

Each NanoPad embeds functionalities such as power supply and digital I/O, leaving very little silicon area available for an analog buffer. Despite the good performances that approaches published in [5]-[10], and [12] offer, to the best knowledge of the authors, none of them fits the space requirements of a NanoPad and the output capabilities that would suit the uIC ball in contact with it. A typical load consists of parasitic capacitances added by the uIC package, the printed circuit board (PCB) metal line and the internal capacitance of the integrated circuit itself. The WaferIC reduces this load because uIC ball lies directly over the NanoPad with no PCB lines which typically introduces an overall load by ~8 pF [12]. It is assumed that total capacitive load that the analog buffer, within the WaferIC, needs to drive is ~12 pF.

In this paper, we describe a compact low-power fast operating analog buffer with configurable slew-rates. As found in an FPGA digital I/O, this novel analog buffer has the capability to adjust its performance according to the load requirements (uIC). The main advantage is power-supply noise injection and total power consumption can therefore be minimized. Section II presents the power supply architecture of the WaferIC and the advantages for a configurable analog buffer. We present in section III the proposed analog buffer and describe the configuration capability. Sections IV and V describe post-layout simulation results and compare our circuit performance with other published works.

II. WaferIC Overview

The WaferIC is a made of a full configurable active 200 mm wafer in a 0.18 µm CMOS technology, which is capable of interconnecting the user integrated circuits deposited on its alignment insensitive surface. To do so the WaferIC can be configured to provide digital/analog links, or act as a regulated power-supply. The following subsections give an overview of the WaferIC topology and its power distribution structure along with the challenges associated with it.

A. The WaferIC architecture

Fig. 1 shows a hierarchical view of the WaferIC where NanoPads are the smallest configurable elements occupying an active area of 77 µm×110 µm. Grouped in Unit-Cell arrays, the NanoPads populate the entire 200 mm Wafer. Each NanoPad is a contact point that can be configured accordingly with the uIC ball that connects it. The WaferIC surface is also covered with an anisotropic conductive film (Z-axis film), which is based on embedded conductive vertical fibers (nickel needles)

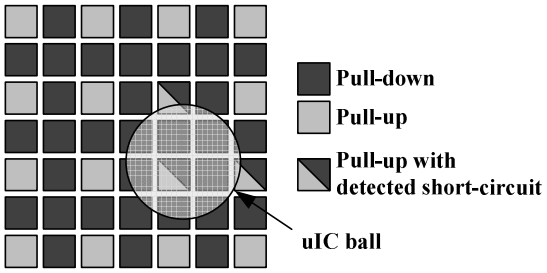

Fig. 2. Contact detection mechanism using weak pull-up and strong pull-down, where detected short-circuits are shown where weak pull-up are absorbed by strong pull-down and causing a detectable anomaly.

[13], to protect the fragile surface of the wafer and to ensure a good electrical and mechanical contact between the NanoPad and the uIC ball.

In order to locate a uIC ball deposited on the WaferIC surface a contact detection mechanism was implemented, by applying a weak pull-up at a NanoPad output and a strong pull-down to its neighbours (Fig. 2). When a uIC ball creates a short-circuit between several NanoPads (minimum 2), the weak pull-up charge would be absorbed and this change can be detected using a XOR gate (detected short-circuits are shown on Fig. 2). The uIC ball position can be deduced by scanning the whole WaferIC surface with a specific sequence and pattern of pull-up and pull-down and then mapping all the detected short-circuits (as in Fig. 2).

B. The WaferIC power distribution network

The WaferIC is powered by two supply rails of 1.8 and 3.3 V, which are the typical supply voltages for 0.18 µm CMOS technology, through an integrated power grid distributed uniformly over the 200 mm wafer. The WaferIC power supply is based on an arborescent topology where a single printed circuit board (PCB) is the root and the NanoPads the leaves.

The main power, which comes from the main AC supply into a 12V DC power supply, travels through specially designed circuit boards called Power-blocks where it is down converted to standard supply voltages of 1.8 and 3.3 V and fed to reticle-images using through silicon vias (TSVs). A Power-block can supply up to 4 reticle-images with maximum current of 5 A and 20 A on 1.8 and 3.3 V rails respectively. The bottom-up

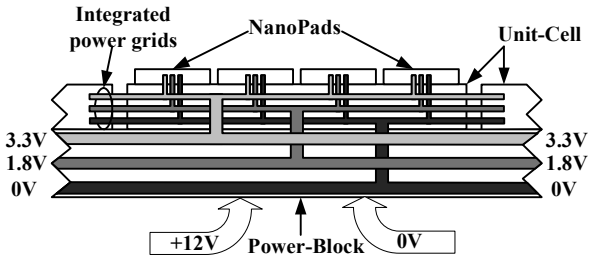

Fig. 3. Power supply distribution of the WaferIC as an arborescence topology.

power flow is shown on Fig. 3.

The integrated grids shown in Fig. 3 are linked through a full reticule-image while the grounds lines are common to the whole WaferIC. Any short on power rail due to defects implies that a full reticle-image circuit have to be disabled. In order to make sure that all circuits are working properly, sufficient voltage headroom must be considered from the root to the NanoPads supplies. Every stage has a DC voltage drop due to parasitic resistances. In our first order model, the main PCB is considered as a perfect electrical conductor because of the metal line thickness and decoupling capacitors. On the other hand, the TSV resistance was measured in [14] to be on average 11 mΩ. The integrated metal grid was chosen to fill the maximum available metal space on the wafer while respecting the design rule check (DRC) of the chosen CMOS technology (0.18 µm). To achieve that, the metal grid dimensions were chosen to be 6 µm in width with pitch of 30 µm [3] [14]. Several combinations of TSV density with the integrated metal density were simulated using COMSOL Multiphysics. A maximum overall acceptable DC drop at the NanoPads grid is 150 mV and the maximum density of TSVs is 1/mm^2. The upper limit of TSVs density is due to a mechanical limitation, where the more holes in the wafer the more fragile it is. The chosen scenario is an integrated metal grid of 6 µm/30 µm (width/pitch) and a 0.25/mm^2 TSV, which gives an overall maximum voltage drop of 90 mV for an equivalent resistance of 257 mΩ [3].

The arborescent power structure combined with the size of the power rails and the number of circuits connected to it makes the power-supply voltages uneven across a reticle-image. This is mainly due to parasitic resistances, process variations or the large number of uIC balls that needs to be supplied and their random placement over the WaferIC surface. These physical and structural constraints could inject significant supply noise in the 1.8 V, 3.3 V and ground grids. The circuits chosen to be integrated within each NanoPad must take those issues into account in order to minimize the supply noise injection.

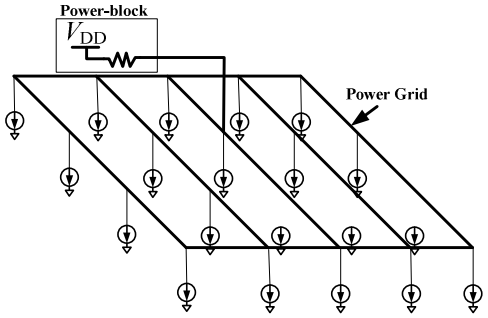

Fig. 4. Simplified worst case model of the WaferIC power grid with an equivalent resistance of 250 mΩ in series with each active circuit (modeled as current source).

III. A Configurable Analog Buffer

Each NanoPad is an independent point of contact, which can ideally receive any type of uIC ball, and act as a regulated power supply, a digital I/O, or analog I/O. The available silicon area, of 77 µm×110 µm is then shared between all those needed functionalities. Existing solutions were already described in [3] for power delivery and the digital I/O footprint was occupying nearly 100 % of the available silicon area. The authors propose in this section a novel configurable analog buffer that fits the very aggressive silicon area requirements of the WaferIC and minimize the noise injection within the power supplies. The proposed solution for integrating an analog buffer has only 21 transistors and yields to a very compact structure of 0.001824 mm^2.

A. *Power supply noise injection*

The size of the WaferIC (200 mm) generates a typically large integrated power grid, which makes supplying all the circuits with a clean power-supply challenging. Any active circuit in any NanoPad or any uIC ball deposited on the WaferIC will induce noise into the power grid. This is due to the fact that the Power-blocks are not ideal voltage sources and that the LDO within can be seen as an ideal voltage source in series with a resistance.

The configurability of the proposed analog buffer is in respect of the main idea of power-supply noise injection diminution. As an explanation, a simplified worst case power-supply grid, which includes an equivalent serial resistance of, for example, 250 mΩ (a typical serial resistance for a discrete linear regulator) from the power supply to the loads, represented as current sources is shown in Fig. 4. A 16 mA loads would create, a DC drop of 4 mV on the power grid. When scaling at the WaferIC level, the noise builds up with the number of operating active circuits. For example, one hundred 16 mA active circuits in parallel would sink 1.6 A with a DC voltage drop equals to 400 mV, which is 2.5 times more than the of 150 mV maximum drop stated in section II. This analysis shows that any active circuits (CMOS circuits connected to the power grid) will inject noise and that this noise needs to be minimized as possible in order to meet the maximum stated voltage drop of 150 mV on the V_{DD} rail.

B. Circuit of the proposed analog output buffer

The proposed analog buffer is made of two complementary and parallel buffer stages (Fig. 5). Both stages work together to boost the output voltage swing. Transistors M1 and M2 from the nMOS stage are matched by M5 and M6 of the pMOS stage. The first buffer is completed by M3 and M4 and the second one by M7 and M8. Each analog buffer is based on a modified differential pairs where the output is tied by M4 and M6 gates, which are diode connected transistors (gate and drain shorted). This allows lowering the output impedance and boosts the buffer speed [11]. Transistor M1 and M2 are simple current mirror (the same for M7 and M8 in the pMOS stage), which ensures that both branches' current are equal allowing *vout* at the gate of M4 and M6 and the gate of M3 and M5 to match *vin*.

C. Small-signal analysis

The output voltage gain A_v of the proposed analog buffer (Fig. 5) can be first estimated from the gain of the nMOS stage. Since both stages are in parallel, the overall gain can be expressed by either the nMOS stage or the pMOS stage when they are sized properly. The small signal analysis of the nMOS stage of the proposed analog buffer is shown in Fig. 6 using the T model, where $id_3 = is_3$ and $id_2 = is_2$. Because both branch current are equal and that M3 matches M4, therefore we can say that $id_2 = -id_3$ and that $gm_3 = gm_4$. The current id_3 can be express by (1) where $g\mathrm{m_n}$ is the transconductance parameter.

$$is_3 = \frac{vin - vout}{1/gm3 + 1/gm_4} = \frac{gm_3(vin - vout)}{2} \tag{1}$$

Output current i_{out} (current at *vout*) of the equivalent circuit shown in Fig. 6 is given by $i_{out} = is_3\text{-}is_2$ and yields to (2).

$$i_{out} = gm_3(vin - vout) \tag{2}$$

Where *vout* can be expressed by $i_{out}\cdot r_{out}$ and where $r_{out} = rds_2//rds_4$ and where rds_n is the drain resistance of transistor M_n, we can write:

$$v_{out} = gm_3(vin - vout)(rds_2//rds_4) \tag{3}$$

Rearranging (3), the voltage gain ($A_v = vout/vin$) of the proposed nMOS stage is obtained and given by (3).

$$Av = \frac{gm_3(rds_2//rds_4)}{1 + gm_3(rds_2//rds_4)} \tag{4}$$

A non-modified differential pair would result in a gain of $A_v = gm_3\cdot rds_2//rds_4$. Equation (4) yield a gain close to unity when $gm_3 = gm_4$ by scaling adequately those transistors. The same approach can be used for the gain of the pMOS stage. When both nMOS and pMOS stages can be made equally matched: i.e. both active stages are in parallel and benefit from each other advantages. In this case, the output voltage swing can be maximized. Equation (5) shows the dependency between the voltage gain Av and the biasing current I_{biasn}. When the slew-rate goes up, so is I_{biasn}, the system becomes faster at the expense of the voltage gain.

$$gm_n = \sqrt{\beta_n I_{D1}} = \sqrt{\beta_n \frac{I_{biasn}}{2}} \tag{5}$$

D. Output voltage swing

The maximum output voltage swing is defined by both the nMOS and the pMOS stages shown in Fig. 5. The nMOS stage stop operating in linear mode when transistors M2 and M4 go out of the saturation region, where $|V_{GS}\text{-}V_{THn}| = V_{DSATn}$ with V_{THn} being the threshold voltage of both nMOS transistors. The minimum voltage drop across M2 is the set to V_{DSATn}, meaning that the upper value of output voltage swing is $V_{DD}\text{-}V_{DSATn}$. On

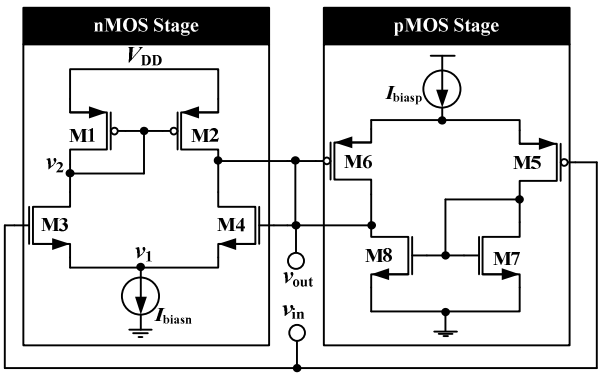

Fig. 5. Proposed output buffer using nMOS and pMOS input transistors in two complementary parallel buffer stages.

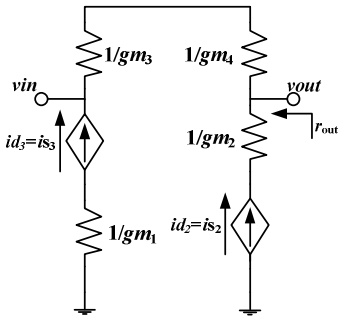

Fig. 6. Simplified small-signal equivalent circuit of the proposed nMOS stage output buffer shown in Fig. 5.

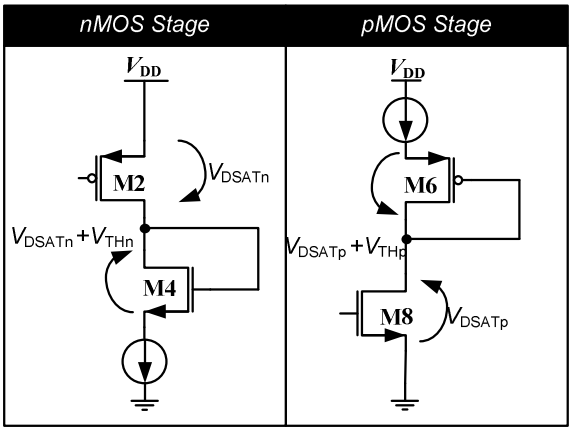

Fig. 7. nMOS and pMOS voltage output swing higher and lower limits of the proposed complementary CMOS analog buffer.

the other hand, the minimum operating voltage of M4 is $V_{DSATn}+V_{THn}$, meaning that the lowest operating voltage is $V_{DSATn}+V_{THn}$ (Fig. 7). The pMOS stage is complementary to the nMOS stage, where the upper and lower limits of the output voltage swing are inverted. The upper limit value is set to V_{DD}-V_{DSATp}-V_{THp} and the lower value to V_{DSATp} (Fig. 7). Combining both nMOS and pMOS stages enhances the maximum output voltage swing by an offset of V_{TH} toward V_{DD} and the ground. The output voltage swing is therefore limited between V_{DSATp} and V_{DD}-V_{DSATn}, with an average value of ~1.4 V for a 180 nm CMOS technology (V_{TH} = ~0.7 V) [16]. The value of V_{DSATx} depends mainly on the transistors sizes and the biasing current, the higher the current: the higher the current, the higher V_{DSATx} is.

E. Configurable slew-rate

Several types of different uIC balls might be in contact with the WaferIC surface with different analog characteristics such as speed, output voltage and load. One method to suit all demands would be to design a buffer with very high performance and current capabilities. However, as discussed in section III, the power supply noise injection is a factor that must be taken into account in wafer-scale integration where there could be several thousands of output buffers. An output buffer that can be configured in terms of slew-rate to match the uIC balls requirements is more desirable for the WaferIC, where the noise injection and power is an issue.

The speed of an analog output buffer is defined by its slew-rate. Augmenting the slew-rate of an analog output buffer can be done by increasing its biasing current [17] at the cost of increased power-supply noise injection, higher quiescent current and the reduction of the maximum output voltage swing. This reduction is due to the fact that V_{DSAT} increases with the biasing current where the drain currents of M2 and M8 (Fig. 5) are

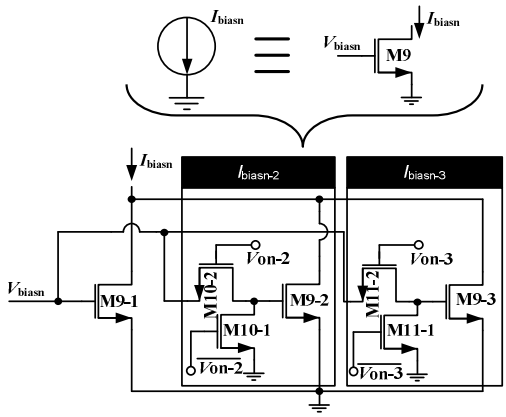

Fig. 8. Proposed slew-rates with a two bits configuration.

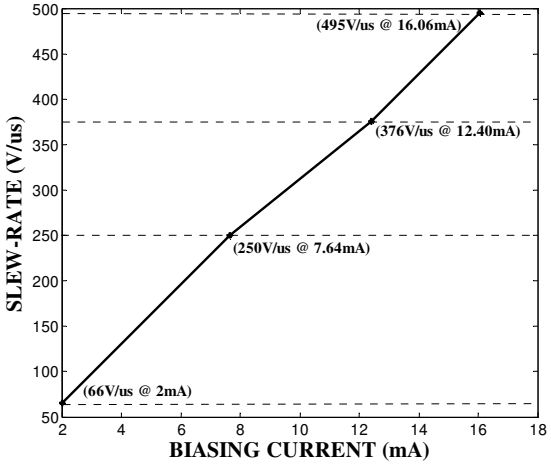

Fig. 9. Proposed biasing current and slew-rates configuration for the complementary CMOS analog buffer.

linked to the biasing current of the analog buffer as shown in (5). The slew-rate configurability is achieved by using an array of nMOS or pMOS (according to the stage) that can be connected or disconnect from the buffer. The current source of nMOS stage of Fig. 5 can be expressed as an nMOS transistor (M9) with its gate biased at a fixed current I_{biasn}, as shown in Fig. 8. This transistor can also be expressed as 3 different transistors with various sizes, M9-1 to M9-3, where M9-1 is always on for a fixed 2 mA I_{biasn} and two control bits (V_{on-2} and V_{on-3}) can enable two other biased transistors. For instance when V_{on-2} is high and V_{on-3} is low, V_{biasn} is connected to the gate of M9-2 (two times the size of M9-1) by transistor M10-2 for an additional 4 mA and M9-3 (two times the M9-2) gate is shorted to the ground by M11-1 disconnecting it from the overall circuits. To make slew-rate of the proposed analog buffer configurable, we propose a biasing current source that can be configured to four fixed values from 2 mA up to a maximum of 16 mA. The needed slew-rates were selected in a linear fashion as shown in Fig. 9.

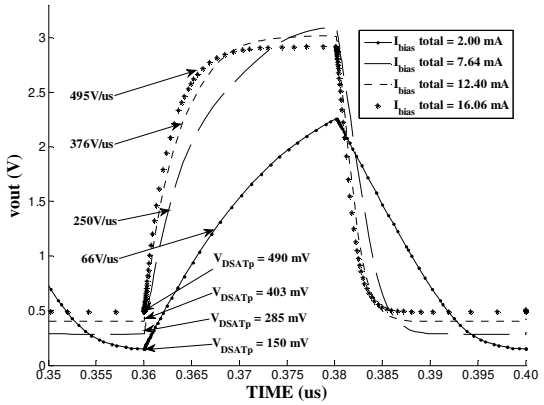

Fig. 10. Output voltage transient response to a 25 MHz square wave of the proposed output buffer with 4 different configurable slew-rates for a 12 pF load.

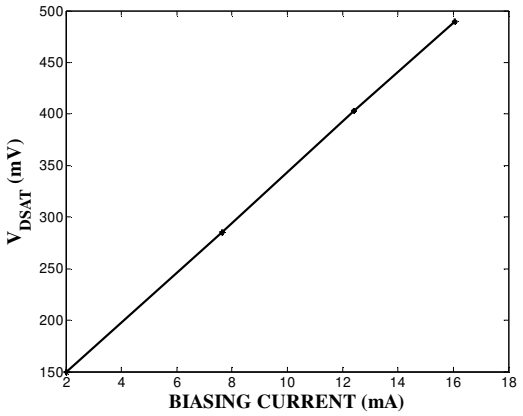

Fig. 11. Relation between biasing current and V_{DSAT}, which set the maximum output voltage swing.

IV. Results and Performance Analysis

The proposed configurable analog buffer has been experimentally validated through post-layout simulations performed in a 0.18 µm CMOS technology. As stated in the introduction section, the WaferIC benefits from an architecture where no metal line are needed to connect the NanoPad to the uIC ball, which drop the overall parasitic capacitance to around 8 pF. For that reason, the following simulations results were extracted with a load of 12 pF.

A. Transient response, slew-rate configuration and output voltage swing

To depict the performances of proposed configurable analog buffer proposed in Fig. 5, transient analysis were done. The worst case scenario of a 25 MHz square wave signal was applied to v_{in} with rising and falling slopes of 500 ps at a maximal amplitude 3.3 V_{PP}. Post-layout simulations shown in Fig. 10 were done throughout all configurable slew-rates, which vary from 66 V/µs, at a biasing current of 2.00 mA, up to 495 V/µs, for a 16.06 mA biasing current.

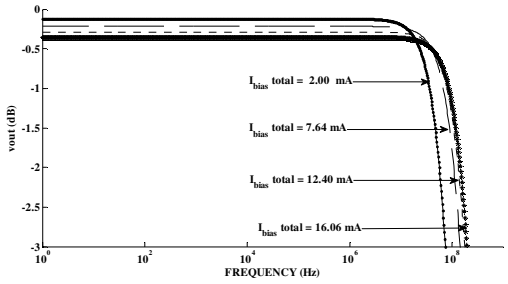

Fig. 12. AC response of the proposed analog buffer for the four configurable slew-rates with a load of 12 pF.

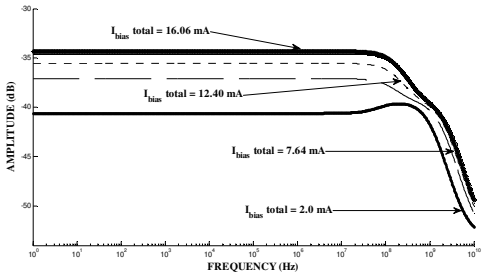

Fig. 13. PSRR of the proposed analog buffer for the four configurable slew-rates with a load of 12 pF.

The output swing follows the theoretical analysis given in section III, where V_{DSAT} is to set the maximum and minimum output voltage swing of the proposed buffer. Fig. 10 shows that for I_{biasn} of 2.00 mA, V_{DSATp} is at its lowest with 150 mV. This value increases linearly with I_{biasn} as shown in Fig. 11 and reaches a maximum of 490 mV at maximum slew-rate as the theoretical analysis predicted it (when I_{biasn} increases so is V_{DSAT}). The output voltage swing is thus a linear relation with the slew-rate. Detailed results are displayed in Table I.

B. AC characterization, power-supply-rejection-ratio and output distortion

The AC response of the proposed analog buffer can be seen in Fig. 12. All configurable outputs confirm what (4) was predicting a voltage gain close to unity. As a result of the choice of topology and the sizing of transistor, the assumption of $gm_3.rds_2//rds_4 >> 1$ can be made, making (4) close to unity. The gain (A_v) is -121 mdB at 66 V/µs and decreases to a minimum of -355 mdB at maximum slew-rate of 495 V/µs. Fig. 12 shows that all the configurations of the analog buffer have a constant gain for the entire operating bandwidth (no ripples). This constant gain ranges from 4.0 MHz (at 66 V/µs) and goes up to ten times more, 40 MHz (495 V/µs). Fig. 12 also shows the -3 dB cut-off frequency, where the minimum and maximum bandwidths are 74 MHz and 194 MHz.

We explained in section III that the WaferIC will suffer from noisy power-supply lines. Taking this into

Table I. PERFORMANCE SUMMARY OF THE PROPOSED CONFIGURABLE ANALOG BUFFER

	Config. 1	Config. 2	Config. 3	Config. 4
I_{bias} (mA)	2.00	7.64	12.40	16.06
Slew-Rate (V/µs)	**66**	**250**	**376**	**495**
V_{DSATp} (mV)	150	285	403	490
V_{DSATn} (mV)	100	200	290	382
Output Swing (V)	3.05	2.815	2.607	2.428
Gain (mdB)	**-121**	**-216**	**-289**	**-355**
PSRR @ 0 Hz (dB)	-40.6	-37.1	-35.5	-35
PSRR @1 MHz (dB)	-40.6	-37.1	-35.5	-35
PSRR @100 MHz (dB)	-39.8	-37.7	-36.1	-35
Settling Time (ns)	142	11.8	7.2	5.
-3 dB bandwidth (MHz)	**74**	**143**	**176**	**194**

account, any circuit using these power supplies has to be as independent as possible from them. The power supply rejection ratio (PSRR) is shown in Fig. 13. The simulations results show that the proposed analog buffer is insensitive from DC to high-frequency noise coming from the power supplies. The low-frequency noise is rejected with more than 40 dB at low I_{bias} = 2 mA (or the smallest slew-rate), and still performs adequately with a -35 dB of PSRR with the largest bias current.. A small ripple can be observed around 100 MHz, which is compensated by the load itself. Fig. 1 depicts DC transfer function for a voltage input that ranges from 0 up to 3.3 V for minimum and maximum slew-rate. As the simulations shows when operating at small slew-rate, the amplitude distortion is minimal as the DC transfer function is almost linear.

The main performances criteria are listed and compared in Table I for all four configurations. The settling time was calculated at 90 % of maximum output swing for a square wave input of 25 MHz as shown in Fig. 10.

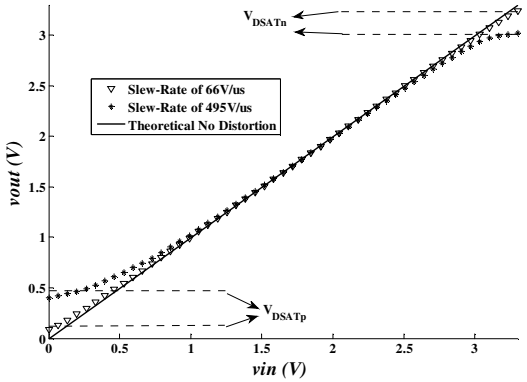

Fig. 1. DC transfer function for minimum and maximum slew-rate configuration compared to the theoretical no-distortion linear output.

Table II presents a performance comparison between existing works and our proposed configurable analog buffer. In order to adequately compare two architectures with different targets and applications regarding operating speed, load and silicon area, a figure of merit (*FOM*) is describe in (6), where the Normalized Area (NA) to 0.18 µm is calculated for a more accurate silicon comparison, the Settling Time (ST) the Load the Voltage Gain (A_v) and the Slew-Rate (*SR*) are the parameters taken into account. The smaller the *FOM* the better the buffer gets. Our proposed configurable analog buffer has a FOM more than 120 times lower than that of a rail-to-rail class-AB CMOS buffer introduced [12]. This factor is mainly due to the very high slew-rate capabilities of the proposed solution.

$$FOM = \frac{NA \cdot ST}{Load \cdot Av \cdot SR} \quad (6)$$

Table II. COMPARISON WITH EXISTING WORKS

	[10]	[12]	This Work
Year	2004	2012	2013
Technology (µm)	0.35	0.35	0.18
Power Supply (V)	3.3	3.0	3.3
Transistor count	26 and R=2k	20	21
Active area (mm^2)	0.00265	0.01460	0.001824
Load (pF)	600	20	12
Gain (dB)	0	0	-0.121 to -0.355
Settling time (ns)	2700	87 ns for a 3 V square wave	5.3 ns for a 3.3 V square wave
Slew-Rate (V/µs)	4.52	81	66 up to 495
-3 dB bandwidth (MHz)	-	5.8	74 to 194
FOM	0.697	0.207	0.00169

V. CONCLUSION

A novel approach using complementary nMOS and pMOS stages architecture of modified differential pairs for a configurable analog buffer has been presented. The introduced buffer can be set to various slew-rates from 66 up to 495 V/µs to suit wafer-scale integration prototyping platform, the WaferIC, where power-supply noise injection and available silicon area are an issue. The proposed analog buffer used only 21 transistors for a total silicon area of 0.001824 mm^2. In addition, the proposed analog buffer has a quasi-unity gain and fast response with a bandwidth that goes up to 194 MHz and a response time of 5.3 ns. This design also achieves a *FOM* better than other designs by a factor of more than 120 times.

ACKNOWLEDGMENT

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ANNEXE C – A Defect-Tolerant Reusable Network of DACs for Wafer-Scale Integration

A Defect-Tolerant Reusable Network of DACs for Wafer-Scale Integration

Nicolas Laflamme-Mayer, Gilbert Kowarzyk, Yves Blaquière, *Member, IEEE*, Yvon Savaria, *Fellow, IEEE,* and Mohamad Sawan, *Fellow, IEEE*

***Abstract*—A novel defect-tolerant network of Digital-to-Analog Converters (DACs) is presented in this paper. The architecture of this converter employs a single 2.5 V voltage reference and an unbalanced buffering technique to achieve a wide voltage range that extends from 864 mV to 2.538 V with an 8-bit resolution. The proposed converter incorporates a defect-tolerant architecture and is extremely compact, utilizing a per-bit silicon area of less than 350 µm^2. Although such very small area allows for embedding in dense configurable fabrics (FPGAs) and wafer-scale integration, the overall performance is not sacrificed as reported measurements show a signal-to-noise ratio of 51.87 dB and a spurious free dynamic range of 42.31 dB, at 10 MS/sec providing 7.6 effective bits. Moreover, the proposed architecture benefits from dynamic calibration capabilities, as any converter output can be finely adjusted over a range of 25 mV. This proposed DAC is also extensively reused in the same defect-tolerant network as for a SAR-ADC, as well as a configurable voltage reference.**

***Index Terms*—Wafer-Scale integration, Network, ADC, DAC, dynamic calibration, defect tolerant, unbalanced, WaferIC**

I. Introduction

Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) are important and even critical components in current electronic designs. They are among the key building blocks that bridge analog and digital circuits. With today's increasing use of mobile devices, there is a growing demand for access to low-cost, low-power, and high-performance ADCs and DACs [1]. Indeed, they are used for carrying out different kinds of data conversions in many types of applications, such as noise rejection, data sampling, power consumption monitoring and biomedical applications [2].

The novel WaferIC prototyping platform introduced in [3] [4] is a good example of a complex electronic system requiring numerous ADCs and DACs. This wafer-scale circuit behaves like a configurable printed circuit board (PCB) that extends over the full surface of a 200 mm silicon wafer (see Fig. 1) [3] [4].

A. ADC Topologies

Several different topologies exist for both ADCs and DACs. Four main techniques to designing ADCs are reported in the literature: *flash, pipeline, successive approximation* and *sigma-delta* (oversampling) [5]. The various approaches can be quantified with a few parameters, such as the resolution (number of bits), the signal-to-noise ratio (SNR), the spurious-free dynamic range (SFDR), the power dissipation and the effective number of bits (ENOB) [5]. We will briefly describe the types of architectures that are currently used for designing ADCs.

The *flash* architecture is parallel in nature, and considered to be the fastest. Nevertheless, it uses 2^{N-1} comparators, where N is the resolution. Because the number of comparators grows exponentially with N, this approach is not energy efficient and employs a very large silicon area, thus making it unusable for wafer-scale integration or embedding in dense configurable fabrics such as FPGAs. Moreover, the numerous integrated components, such as resistor-ladders, make layout matching challenging and have limited this approach to building ADCs having up to only N=9 bits of resolution [5][6].

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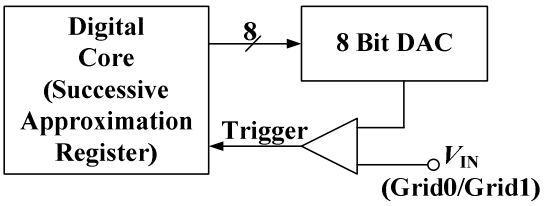

Fig. 2 Typical SAR-ADC architecture.

The *pipeline* ADC architecture is mostly used in high-speed applications, such as wideband receivers, where the power consumption is to be considered [7]. Pipeline ADCs are often implemented using switched-capacitor circuits, and their overall performance depends on the required operational amplifiers (op-amps) and the size of the capacitors used: the larger they are, the better the matching can be, but this is done at the expense of an increase in power consumption and silicon area [7]. The integration of such numerous large capacitances also makes this approach unsuitable for use in the WaferIC.

The *delta-sigma (ΔΣ)* architecture uses digital circuit blocks instead of analog ones, and trades speed for overall resolution by sampling the input signal at a rate several times larger than the Nyquist rate [5]. Switched capacitor networks are widely used as building blocks for the architecture, which makes the ΔΣ-ADC larger to integrate [8]. A solution minimizing the number of integrated passive components and offering signal integrity over large silicon distances (full 200mm wafer) is necessary for use with the WaferIC, thus excluding the ΔΣ-ADC architecture as a viable option.

The authors in [9] explored a solution using an asynchronous delta-modulator based architecture as a solution. This proposed approach is however targeted for a moderate bandwidth of 2 MHz.

Successive Approximation Register (SAR) based ADCs have a small silicon area footprint and a low-power consumption, since, compared to the other approaches, the converter only requires a single signal path with one comparator. It offers a high resolution in exchange of conversion speed. The total conversion cycle is spread over several clock cycles, in which the input signal is compared with a reference level delivered by a DAC [6]. A SAR-ADC is composed of three distinct modules (Fig. 2). The first module is a digital controller, which asserts the second module, a DAC. The third module is a comparator that generates a *Trigger* signal after determining whether the input V_{IN} (signal to sample) is equal to the value produced by the DAC [6], [10], [11]. The size and performance of the SAR-ADC mostly depends on the switched capacitor or current steering DAC employed [6].

B. DAC Topologies

Digital-to-analog converters are typically based on either *current-steering*, a *charge scaling technique* or a *resistive ladder*. The *current-steering* topology requires a large number of distinct and matched current sources, which significantly impacts the resulting silicon area. Indeed, as shown in [12], the required silicon area for a binary-weighted current steering 10 bits DAC is 4 times larger than the available surface for a full NanoPad. Other designs have been published in [13] and [14], but none have a silicon area comparable to or less than that of a NanoPad.

The *charge scaling technique* requires a large number of integrated passive components that need to be matched. None of the published topologies offer a small-enough silicon area such that it could be used for wafer-scale integration into the WaferIC [15], [16].

Since the WaferIC integrates over 1.2 million NanoPads, and each NanoPad has to be able to access both ADC and DAC functionalities, a large number of integrated converters is required. To the best of our knowledge, no existing design or topology allow for wafer-scale integration within the silicon area and power budget available on the targeted platform.

In this paper, a SAR-ADC architecture is proposed. It employs a novel DAC based on an unbalanced buffering technique. The DAC does not require switched capacitors or current steering techniques, and only uses a single 2.5 V voltage reference to generate 256 different voltage levels. Using this novel architecture, 300 thousand of these ADCs/DACs can be integrated into a defect-tolerant network that is suitable for wafer-scale integration. The addition of ADCs and DACs to a platform such as the WaferIC enables support for a wider range of applications, such as internal/external signal sampling, analog signal generation, and interfacing with analog busses. Furthermore, it allows for processing and generating analog signals, sampling, and providing analog bus functionality.

In order for this addition to be effective, ADCs and DACs have to be accessible from each and every one of the 1.2 M NanoPads, which is a challenge in terms of minimizing the total resulting silicon area. Moreover, wafer-scale integration requires the use of redundancy and defect-tolerant architectures since no fabrication process has a yield of 100%, particularly at that level of integration. Therefore, we propose the use of a defect-tolerant network of ADCs and DACs: over 300 thousand converters are shared between all NanoPads. The proposed ADCs/DACs are based on an unbalanced buffering technique that yields a very compact silicon area. Combined with the proposed sharing network, they

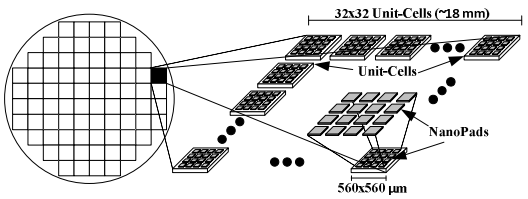

Fig. 1 The WaferIC is composed of a same 32×32 matrix of Unit-Cell that is photo-repeated 76 times over the surface of the whole wafer.

allow for any defects to be overcome by re-routing the faulty ADC/DAC functionalities to a working set of ADCs/DACs. The same DACs are also employed in the ADC structure, and their per-bit silicon size of 350 μm^2 does not compromise performance. Indeed, at 10 MS/s, SFDR of 41.31dB and an ENOB of 7.6 bits were measured.

The paper is organized as follows: Section II focuses on the proposed small-area DACs, which are also employed in the proposed Successive Approximation Register based ADCs (SAR-ADCs). The implemented defect-tolerant ADC/DAC network is described in Section III. In Section IV, experimental results obtained from a test chip implemented using 0.18µm CMOS technology are reported, and in Section V the proposed solution is compared with other recently published ADC/DAC architectures.

II. A DAC Architecture Based on Unbalanced Buffer

Conventional DAC structures mainly employ switched capacitor networks or current steering techniques. Integrating and matching a large number of either capacitances, current sources or other passive components has a large impact on the silicon area, and thus determines whether they can be integrated within the WaferIC or not.

In this section the proposed DAC is presented. This circuit is adapted from the analog buffer in [18]. The characteristics of an implemented solution are reported and means to maximize the output range while minimizing the silicon area are explored.

A. A multi-reference voltage-level generator

The three-stage circuit presented in [17] (see Fig. 3) employs a configurable unbalanced differential pair for generating a range of output voltages. The first stage of this circuit uses a conventional bandgap generator (BGR) to provide a stable 1.5 V reference voltage that is insensitive to temperature and power-supply variations. The second stage employs this single voltage reference to generate a range of 246 distinct voltage levels, each at around a 10 mV step increment. This is achieved by selecting the transistor ratios in the unbalanced differential pair in order to shift the reference voltage up or down. In the third stage the generated output voltage from the second stage is buffered, to allow driving a larger load at V_{OUT} (see Fig. 3). From [17] the expression of V_{OUT} is given by (1)

$$V_{OUT} \propto \sqrt{W_3 L_4 / W_4 L_3} \tag{1}$$

If we were to vary both M3 and M4 to widen the unbalancing capabilities, offsetting the 1.5V reference both down and up equally, this approach would be plagued by the non-monotonous output voltage V_{OUT}. It would require the use of a digital decoder where the digital '0' would be 1.5V, '-128' the lowest value such as '1.5V-*X*mV' and '+128' the highest value at '1.5V+*X*mV'. The approach used in [17] sets M3 ratio (*W/L*) down to achieve lower output voltages of that the voltage reference of 1.5V. Then M4 ratio is scale up properly to increase V_{OUT} from 1.33V (digital 0) up to 3.04V (digital 256). M3 could be scale down deeper to achieve lower value at the cost of a large increase of M4 silicon area.

B. Proposed unbalanced buffer

When speaking of Wafer Scale integration, such as in the WaferIC, the used silicon area is one of the foremost criteria. Using circuits that can be reused several times or reconfigured to achieve different functionalities is crucial. The proposed unbalanced buffer is a structured intended to be used as a 1:1 analog buffer, a DAC, a SAR-ADC, and a configurable voltage reference. We will focus in this paper on its capabilities of a DAC, and a voltage configurable voltage reference.

In this paper, a novel approach is proposed for improving the multi-stage level generator shown in Fig. 3. Indeed, it employs a similar approach as that of [17] by combining it with the configurable and compact analog buffer presented in [18] (Stage #3), and enhances it to eliminate its non-monotonic nature and combines it with Stage #2, thus increasing its driving capability and its output voltage range.

The analog buffer in [18] uses a modified differential pair comprising complementary nMOS and pMOS stages to achieve a wide output range. Fig. 4 shows a transistor-level schematic of this buffer. M1 and M2 form a simple current mirror while M3 and M4 are the modified differential pair. When M1 has the same size as M2, and M3 has the same size as M4, if we neglect the channel modulation and assume that all transistors are in their saturation region, I_1 and I_2 can be approximated by (2) and (3) respectively:

$$I_1 = \frac{\beta_3}{2}\left(V_{IN} - V_2 - V_{THN}\right)^2 \tag{2}$$

$$I_2 = \frac{\beta_4}{2}\left(V_{OUT} - V_2 - V_{THN}\right)^2 \tag{3}$$

where β_X is the transconductance parameter of transistor x. Note that when the circuit in Fig. 4 is balanced, $\beta_1 = \beta_2$ and $\beta_3 = \beta_4$, thus $V_{OUT} = V_{IN}$.

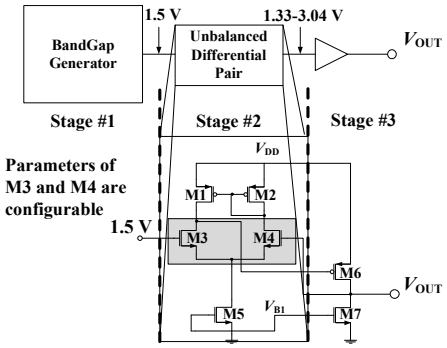

Fig. 3 Unbalanced differential pair using a single 1.5 V voltage reference to generate 246 output voltages at 10 mV step-intervals, ranging from 1.33 to 3.04 V [17].

The circuit in [18] was modified to employ an enhanced unbalanced circuit as of in [17]. Indeed, the resulting circuit implements an ultra-compact 8-bit DAC (Fig. 4). Note that V_{OUT} depends on I_1 and I_2, which are approximated by (4) and (5) as follows:

$$I_1 = \frac{\beta_1}{2}\left(V_{DD} - V_1 - V_{THP}\right)^2 \tag{4}$$

$$I_2 = \frac{\beta_2}{2}\left(V_{DD} - V_1 - V_{THP}\right)^2 \tag{5}$$

Therefore, neglecting the channel modulation, the value of V_{OUT} can be approximated by first equaling (2) to (4) and (3) to (5), such as to isolate V_1 as shown by (6) and (7) below.

$$V_1 = \sqrt{\frac{\beta_3}{\beta_1}}\left(V_{IN} - V_2 - V_{THN}\right) + V_{DD} + V_{THP} \tag{6}$$

$$V_1 = \sqrt{\frac{\beta_4}{\beta_2}}\left(V_{OUT} - V_2 - V_{THN}\right) + V_{DD} + V_{THP} \tag{7}$$

Then, assuming all transistors are in saturation region and that transistors M3 and M4 have an equal size (i.e. $\beta_3 = \beta_4$), by equaling (6) to (7) and isolating V_{OUT}, (8) can be obtained.

$$V_{OUT} = \sqrt{\frac{\beta_2}{\beta_1}}V_{IN} + \left(1 - \sqrt{\frac{\beta_2}{\beta_1}}\right)\left(V_2 + V_{THN}\right) \tag{8}$$

Nevertheless, as the V_{OUT} voltage increases, depending on the size of M2, V_{DS2} may fall below the value of V_{DSAT}, the voltage necessary for M2 to remain in the saturation region, thus placing the transistor in its triode region. The current flowing through M2 would then be given by (9), and V_{OUT} can then be approximated by (10) below.

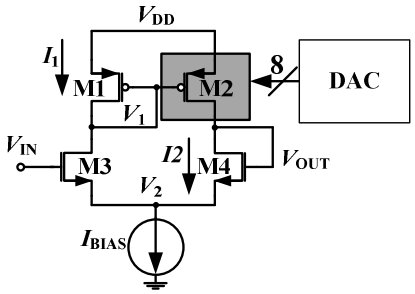

Fig. 4 The simplified schematic of the 8-bit configurable analog buffer based on [18], and which replaces Stages 2 and 3 in Fig. 3.

$$I_2 = \beta_2\left(V_1 - V_{DD} - V_{THP}\right)\left(V_1 - V_{DD}\right) - \frac{\left(V_1 - V_{DD}\right)^2}{2} \tag{9}$$

$$V_{OUT} = \sqrt{\frac{2\beta_2}{\beta_4}}\sqrt{\frac{\beta_3}{\beta_1}\left(V_{IN} - V_2 - V_{THN}\right)^2 - \sqrt{\frac{\beta_3}{\beta_1}}\left(V_{IN} - V_2 - V_{THN} - V_{TH}\right.} \ldots + V_2 + V \tag{10}$$

Equations (8) and (10) reveal the V_{OUT} dependency on all transconductances β_x, thus allowing several degrees of freedom for unbalancing and configuring the output voltage. Indeed, by looking at (8) and (10), the common βx terms in both equations would be β_1 and β_2 (since β_3 only appears in (10)). Using variables β_1 and β_2 to configure the circuit would make the design simpler, since V_{OUT} can then be expressed using a common set of terms for (8) and (10). Increasing the width of M1 would result in an increase of β_1, thus resulting in a lower V_{OUT}. Increasing its length would result in the opposite effect (i.e. an increased V_{OUT}). Conversely, varying the width and length of M2 would have a complementary effect. However, only β_2 is present in (8) and (10) with the same exponent (i.e. $\beta_2^{(1/2)}$) and therefore using it (instead of β_1) for configuring the circuit greatly simplifies the transistor size selection, thus allowing for a more regular growth of the resulting V_{OUT}. Nevertheless, selecting M2 as the transistor for unbalancing the circuit allows several scenarios. Some of these scenarios may improve the voltage range, while others may reduce the silicon area, or the number of necessary reference voltages (V_{IN}).

C. Proposed technique to set the overall output range

In wafer-scale integration, particularly for the WaferIC, the most important criteria for selecting a design over another is the silicon area employed and the maximum output voltage range achieved. Indeed, the objectives are to minimize the *silicon area* and *maximize the output voltage range*. To that end, different possible scenarios for obtaining a compact yet flexible DAC are considered.

When using the proposed buffer-unbalancing technique, the appropriate V_{IN} reference voltage and an

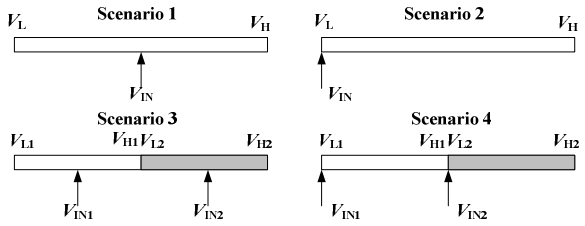

Fig. 5 Proposed scenarios to range a single V_{IN} into several V_{OUT}.

effective output range must be selected. Ideally, transistors M1 to M4 in Fig. 4 should always be in saturation to ensure that (9) remains valid. Therefore, M3 and M4 must be equal in size, leaving M1 and M2 to be adjusted and configured. Recall that as M1 is sized larger than M2 (i.e. $\beta_1 > \beta_2$), V_{OUT} decreases. Conversely, as M1 is sized smaller than M2, V_{OUT} increases.

Four scenarios are proposed, each providing a different output linearity, output voltage range and silicon area usage.

In the first scenario, V_{IN} is initially chosen such that it is equal to the center value of the expected output voltage range. Then, by resizing both M1 and M2, the value of V_{OUT} can be configured down to V_L (voltage low) or up to V_H (voltage high). Indeed, whereas increasing the width of M1 moves V_{OUT} toward V_L, increasing the width of M2 moves V_{OUT} toward V_H. Finally, when both M1 and M2 are equal in size, $V_{OUT} = V_{IN}$. However, to ensure its monotonicity, a digital encoder is required as in [17] and detailed in section II(a). Another approach of the one used in [17] is proposed. To increase V_{OUT} higher than V_{IN}, M2 ratio (*W/L*) needs to increase while keeping M1 ratio constant, or the other way around to make V_{OUT} lower. In a 8-bits configuration the logical '0' would be when V_{OUT}=V_{IN}. Then the 4-LSB (Least Significant Bit) would move V_{OUT} toward its minimum value reaching it at the digital code "1111". To increase $V_{OUT} > V_{IN}$ the 4-MSB would then be used while maintaining the 4-LSB at "0000". This approach severely impacts the required number of bits since 8-bits would give and overall 64 different V_{OUT} as well as needing also a digital decoder. Doing otherwise would negate the monotonicity where several voltage intervals would interlace with one another.

The second scenario, consists in employing a fixed V_{IN} value, locked at V_L or either V_H. In this case, the full output voltage range is obtained by resizing M2 up or down to range V_{IN} up or down depending on the designer choice. A lower V_{IN} value may be attained by using a low-voltage BGR, or by fixing the size of M1 to a larger value.

Scenarios 3 and 4 are similar to Scenarios 1 and 2, but use two V_{IN} values rather than one fixed V_{IN}. The output range for each V_{IN} and the overall configurable size of M1 and M2 are then reduced. The advantage offered by Scenarios 3 and 4 is that smaller M1 and M2 transistors can be used to obtain the same overall V_{OUT} voltage range. Nevertheless, this is achieved at the expense of having to generate multiple references, which is costly in terms of silicon area. Moreover, this approach makes the monotonicity hard to achieve when switching from one reference to another while keeping the step sizes small and constant. It would require a very precise voltage references as well as very small offsets.

Table I summarizes and compares the main characteristics of the four proposed scenarios. As can be seen, Scenarios 3 and 4 require multiple V_{IN} references, each generated from a different BGR, which typically require parasitic PNP transistors having prohibitively large silicon areas. We can also observe that Scenario 1 may be unsuitable and is not the best in the target application as its monotonicity would require a digital decoder as well as only offering 64 V_{OUT} with an 8-bit configuration. Therefore, given that *minimizing the silicon area* and *maximizing the output voltage range* main selection criteria, Scenario 2 was chosen for implementing the DAC. The non-linear output voltage range observed for Scenario 2 is not as critical, given that the DAC is to be used in SAR-ADC solution. Indeed, this non-linearity is compensated in an analog bus (ADC to DAC), since the same DAC would be used for the input (i.e. data sampling) and the outputs. Moreover, since the transfer function of the proposed DAC is known, (see (8) and (10)), it is possible for the user to linearize the output when necessary. The key message to remember is that while the chosen design, Scenario 2, offers a monotonic output voltage range and only involves a single reference voltage, its full range of generated output voltages is not linear.

The effective width of M2 can be adjusted by varying its 8-bit digital input code (see Fig. 4). Fig. 6 depicts the simulated V_{OUT}, as a function of (8) and (10), for different widths of transistor M2 and a fixed M1 transistor width. Each plotted line represents a per-bit width of M2, chosen as a multiple of a factor *K* (where *K* is an integer ranging from 1 to 255) with the minimal transistor width *U*. Thus, for each digital input code bit-increase, the effective width of M2 grows by $K \cdot U$. Fig. 6 also shows the overall output voltage linearity obtained with the proposed technique. As can be observed, the more M1 and M2 are unbalanced, that is, the more different their widths are, the less linear the full output voltage range becomes.

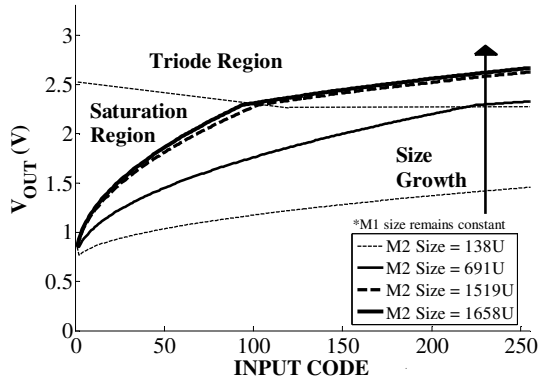

Fig. 6 Simulated DAC voltage as a function of its digital input code, for different widths of M2 and while employing a single BGR voltage reference.

Table I. Comparison of the 4 proposed scenarios.

	Scenario 1	Scenario 2	Scenario 3	Scenario 4
M1 and M2 Sizes	Medium	Large	Small	Medium
# of V_{IN} References	1	1	2	2
Overall Silicon Area	Large	Medium	Large	Large
Monotonicity	YES (with decoder)	YES	NO	YES
Linearity on the full V_{OUT} range	NO	NO	YES	YES

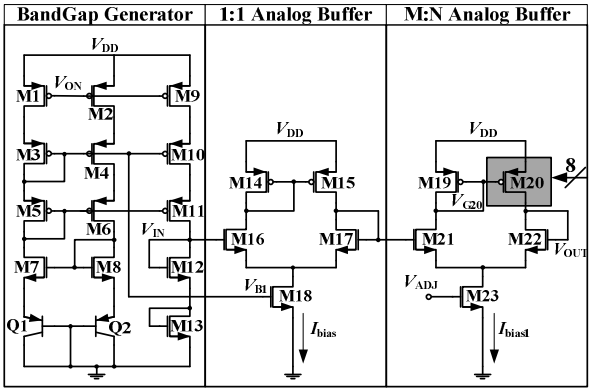

Fig. 7 Proposed solution for generating analog voltages using an unbalanced buffer technique.

D. Proposed DAC using the unbalanced buffer technique

The proposed circuit shown in Fig. 7 includes 3 distinct stages. The first stage is a BGR, the second is a 1:1 analog buffer, and the third is the proposed unbalanced buffer (Fig. 7).

The BGR is adapted from [17]. A Proportional To Absolute Temperature (PTAT) current is created through M3 and M8, and then it is duplicated by M10 and M11. A cascode current mirror was chosen to obtain a better V_{DD} noise isolation. The PTAT current is then pushed into diode-connected transistors M12 and M13, which are Complementary To Absolute Temperature (CTAT).

Transistors M1, M2 and M9 are on/off switches controlled by V_{ON} to enable or disable the circuit. Proper current management is important in wafer-scale integration: since the proposed wafer-scale circuit is populated with over 300k ADCs and DACs, their currents quickly add up. For example, if all 300k ADCs and DACs were always kept on, a quiescent current of 100 µA per circuit would result in a total of 30 A of potentially wasted current. Therefore, having the ability of independently turning specific circuits on and off is mandatory.

The expression for V_{IN} is given by (11). Assuming both drain currents are equal (i.e. $I_{D12} = I_{D13}$) (12) can be obtained. The temperature behavior for each term in (12) is express in (13). By properly adjusting I_{D12}, V_{IN} can become insensitive in the first order to temperature variations.

$$V_{IN} = V_{GS13} + V_{GS12} = \sqrt{\frac{2I_{D13}}{\beta_{13}}} + \sqrt{\frac{2I_{D12}}{\beta_{12}}} + 2V_{THN} \quad (11)$$

$$V_{IN} = 2V_{THN} + \sqrt{2I_{D12}}\left(\frac{1}{\sqrt{\beta_{13}}} + \frac{1}{\sqrt{\beta_{12}}}\right) \quad (12)$$

$$V_{IN} \propto \text{CTAT+PTAT} \quad (13)$$

The 1:1 analog buffer in the second stage shields the bandgap generator from the M:N analog buffer. Indeed, the 8-bit addressable transistor M20 can inject noise on the gate of M21. The BGR in the first stage is not designed to sustain this type of noise, nor is it designed to drive a large current. The use of this buffer isolates the first and third stages, and ensures that the proposed DAC in the third stage remains stable and able to offer a high-bandwidth.

In order to obtain a 1:1 analog buffer that is insensitive to temperature variations, I_{BIAS} needs to be CTAT (see Fig. 7). The electron mobility of a transistor decreases as the temperature increases, thus decreasing the drain current of a transistor. In counterpart, the threshold voltage (V_{TH}) has a CTAT effect on the current: at lower V_{GS} as the transistor mobility effect dominates, making the overall drain current PTAT; the opposite occurs at higher V_{GS}, making the drain current CTAT [19]. By using M18 as a bias current source with its gate connected to V_{B1}, the I_{D18} current is ensured to be CTAT since its V_{GS18} remains at a higher voltage (~2.5 V), thus helping the 1:1 analog buffer to achieve temperature independence. V_{IN} has been set to an output voltage of 2.5 V and will be varied down to ~850 mV, as per Fig. 6.

The final stage is the configurable M:N analog buffer. Only transistor M20 is configurable in size, such as to lessen the silicon area requirements. Scenario 2 was

selected (see Fig. 5), to reduce V_L down to 0.85V from the 2.5 V BGR generated voltage (V_{IN}). Indeed, the size of M19 size was chosen such that this targeted lower voltage value could be reached. Using this technique, the chosen M1 and M2 sizes allow V_{IN} to be varied from 0.85 V to 2.5 V with an 8-bit resolution (maximum range). The widths of the 8 transistors constituting M20 range from a minimum-sized transistor width in the 0.18µm CMOS technology employed (i.e. $W_{MIN} = 0.42$ µm) to a maximum width of $128 \times W_{MIN}$, using a quadratic growth for each addressable bit (i.e. a doubling of the width for every additional addressable transistor). The result is a linear increase of M20's size from W_{MIN} to $256 \times W_{MIN}$ with W_{MIN} steps.

To mitigate process variation effects and to improve the matching between pairs of ADC-DAC converters in the WaferIC, a dynamic calibration method is also proposed. The DAC's bias current can be adjusted using the V_{ADJ} signal at the gate of M23 (see Fig. 7), thus varying the V_{OUT} output voltage up or down as required. Using this method, the circuit can compensate for process variations, mismatches, and even temperature or V_{DD} variations, since V_{OUT} depends on I_{BIAS1} as demonstrated in (9).

The aim of this paper, as mentioned in previous sections, is to reuse the proposed configurable analog buffer as a DAC, a configurable voltage reference, as part of a SAR-ADC and as a 1:1 analog buffer. Thus, the calibration of V_{ADJ} would be done by a neighboring DAC used as a configurable voltage reference. The setting of V_{ADJ} within the WaferIC could be done using its contact detection mechanism [4], where a pull-up of 1.8V can be applied at any NanoPad. Using this known reference, V_{ADJ} can then be tuned to match that 1.8V reference with its known corresponding digital equivalent code of the DAC.

The size of M20 can be configured through a combination of switches. A first configuration technique, presented in Fig. 8(a), consists in employing a transistor switch M20-2A in series with another transistor, M20-1A, whose gate is connected to M20 (i.e. V_{G20}). This technique divides the overall desired M20 size over several parallel switch-branches that can be independently enabled or disabled. Nevertheless, since M20-2A is in its triode region (i.e. having a small drain resistance), this technique is hard to adjust properly.

A second approach, presented in Fig. 8(b), is similar to the one proposed in [21] and uses minimum-size transmission gates (M20-3B and M20-4B) in parallel with a complementary minimum-size pull-up. Transistor M20-1B has an $M \times W_{MIN}$ size. When V_{ON} is set to a logic high, the transmission gate connects the gate of M20-1B to V_{G20}; conversely, when V_{ON} is set to a logic low, it shorts the gate of M20-1B to V_{DD}, thus turning the path through M20-1B off and disabling M20-1B's

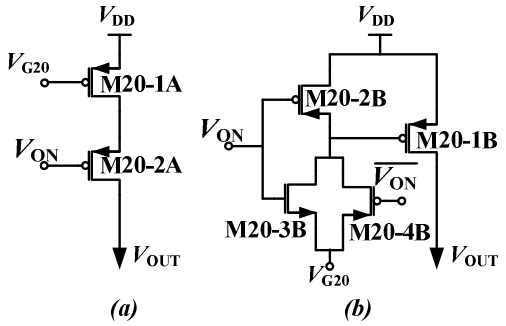

Fig. 8 (a) Serial technique for changing M20 overall transistor size (Fig. 7). (b) Parallel technique with transmission gate and pull-up used to change the overall transistor size.

contribution to I_{20}. This second approach is faster than the first approach, since M20-2B, M20-3B and M20-4B are minimum-size transistors, whereas the serial technique in Fig. 8(a) employs a M20-2A transistor having a size comparable to M20-1A ($M \times W_{MIN}$).

III. A Fault Tolerant Network of ADCs and DACs

A. Proposed ADC-DAC architecture for a Unit-Cell

Any wafer-scale or large area integrated circuit (LAIC) must be defect tolerant to mitigate fabrication process defects. Because of the very large number of NanoPads (>1.2 M) and the fact that each pad must have access to both ADCs and DACs, a carefully planned architecture is proposed. The geometry of the WaferIC dictates that only two NanoPads with independent functionality can be operated at the same time within a Unit-Cell [3], [4]. Taking this into account, an architecture is proposed in which two ADC and DAC pairs are placed in parallel within each Unit-Cell. The ADC-DAC pairs are interconnected using a sharing network, such as to mitigate the impact of manufacturing defects in the WaferIC.

B. Proposed defect-tolerant resource sharing network

Unit-Cells are divided into two independent halves, each having one ADC, one DAC, serving eight NanoPads (see Fig. 1 and Fig. 9). Within a same Unit-Cell half, NanoPads may access either the ADC or DAC functionalities, but never both at the same time. The left half Unit-Cells share a common integrated metal and tri-state buffer grid, labeled GRID0. Likewise, the right-half Unit-Cells share GRID1 (see Fig. 9).

Fig. 10 shows how GRID0's integrated metal lines connect to the ADC and DAC within a Unit-Cell's left half using software-controlled tri-state analog multiplexers. An ADC's input may either arrive from its corresponding NanoPads, or from NanoPads that are located on the same grid, either East or West of that Unit-Cell. Indeed, software-controlled transmission

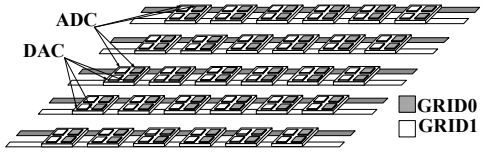

Fig. 9 Proposed network for sharing ADCs and DACs over the full WaferIC.

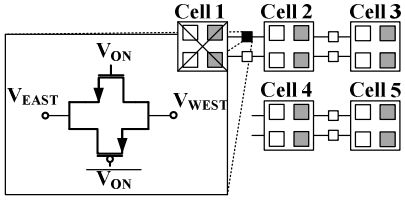

Fig. 10 Transmission gate network allowing east/west analog signal propagation, given a faulty Unit-Cell 1.

gates determine how signals between Unit-Cell halves on a same grid can propagate (see Fig. 12). For example, if a uIC ball's signal needs to be sampled by any of the NanoPads on Fig. 12, its corresponding analog buffer will propagate the signal to the nearest functioning ADC. This may either be the ADC corresponding to the NanoPads in contact with the uIC ball, or the first working ADC located either East or West on the same grid. Likewise, the DAC's output may either be sent through a tri-state analog buffer to the left-half Unit-Cell's NanoPads, or to a set of NanoPads located East or West on the same grid. Note that the DAC's generated signal is simultaneously output to all the NanoPads on a same Unit-Cell half.

GRID0 and GRID1 each implement a defect-tolerant network (see Fig. 9 and Fig. 11), since they allow for NanoPad signals to skip faulty Unit-Cells and be routed to the closest functioning ADC or DAC. In its current form, due to silicon-area constraints, the defect-tolerant network was only extended horizontally (East to West), but in theory it could additionally be extended in the vertical direction (i.e. North to South).

Fig. 10 shows a set of five Unit-Cells distributed onto two rows. In this example, the objective is to either sample or generate a signal on Cell 1's NanoPads. Nevertheless, Cell 1 is faulty. Under normal circumstances, the ADC or DAC within this Unit-Cell would accomplish this task, but given that it is faulty, the proposed network allows for propagating the signal to its eastern neighbor's DAC or ADC through the use of a transmission gate. Using this technique, Cell 1 NanoPads will be able to employ the converters in Cell 2 to accomplish the task. Forwarding an analog signal requires an exclusive access of the grid segment between the faulty cell and the cell replacing its functionality, but it allows for the other Unit-Cells to remain otherwise untouched. Moreover, when forwarding analog signals, more than one faulty cell may be skipped. Indeed, the best-case scenario, for a reticle-image comprising an array of 32×32 Unit-Cells where every converter is operational, 32×2 ADCs or 32×2 DACs per row are available. Therefore, NanoPads above a faulty Unit-Cells can be wired to any of the up to 31 available alternative ADCs or DACs on the same grid.

IV. Results

A. Die of test chip and layout

The test chip, manufactured using a 0.18 µm CMOS technology, is shown in Fig. 13. Each Unit-Cell is 560 µm ×560 µm in size and the NanoPads are 77 µm ×110 µm in size. The rest of the silicon area is employed for other digital components that are essential for the WaferIC, such as the JTAG chain for configuration. This buffer was design to be able to drive a capacitive load of 1 pF. The DAC's active silicon area measures 72.5 µm × 38.4 µm (0.00278 mm^2), which is roughly one third of a full-sized NanoPad. Within the DAC, the configurable unbalanced buffer accounts for 0.00132 mm^2, representing half of the active area, while the remainder is occupied by the BGR and the 1:1 analog buffer.

B. DAC characterization

The proposed DAC was validated experimentally for all 256 possible digital inputs values, and their corresponding output voltages, ranging from 864 mV up to 2.538 V, are shown in Fig. 15. The DAC output is monotonic, with a LSB step that ranges from 100 µV to 24 mV and an average LSB of 5.6 mV. Fig. 15 also shows that the predicted V_{OUT} from (8) and (10) follows the experimental results, and that M2 falls into the triode region around a digital input of 95 to 140 (as per Fig. 6), for a corresponding output voltage ranging between 2.1 and 2.35 V.

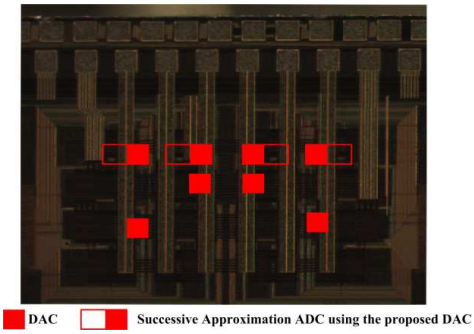

Fig. 13 Die of test chip: two Unit-Cells are shown, comprising a total of 4 DACs and 4 SAR-ADCs.

The Differential Nonlinearity (DNL) of the DAC, shown in Fig. 16, was computed using the calculated LSB from (8) and (10). Normally the DNL is measure using a straight line. However, as mentioned before the proposed configurable analog buffer used as a DAC do not offer a linear output. Thus, comparing its response with a straight line would not reflect the overall

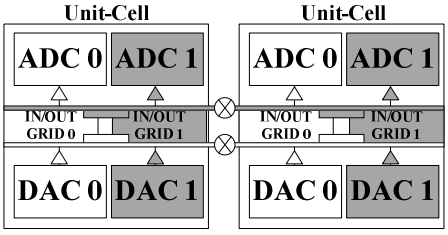

Fig. 11 Unit-Cells are composed of two independent halves, each having one ADC and one DAC. Unit-Cell left-halves are connected to GRID0 and Unit-Cell right-halves are connected to GRID1.

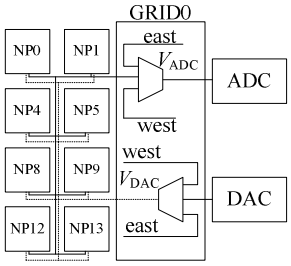

Fig. 12 A Unit-Cell's left-half ADC input is either connected to its own NanoPads, or to NanoPads connected to GRID0 on a neighboring cell to the East or to the West of the given Unit-Cell. Likewise, its DAC output is connected to either its own NanoPads, or to NanoPads on a neighboring cell to the East or to the West on GRID0. Note that a Unit-Cell half either enables the ADC or the DAC (but not both at the same time).

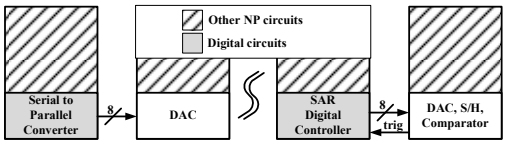

Fig. 14 Layout floorplan of the proposed SAR-ADC and DAC network within a Unit-Cell

accuracy of the proposed DAC.

The measured DNL of the presented DAC has an overall average DNL of 0.41 LSB. A clear break can be observed at the digital input value of 113: this is due to M20 (see Fig. 7) entering its triode region, thus increasing the DNL. Below a digital input of 113, the average DNL is equal to 0.163, which is an improvement by a factor of 4. By using a scenario where several V_{IN} would have been used, thus M20 would never leaves the saturation region, as is described in Section II.C, which would have greatly improved the DNL when the digital input value is over 113.

Notice that, as shown in Fig. 15, this proposed DAC is not linear and the INL measurement of only the DAC would not be representative and not fit for the requirement of the WaferIC. Be aware that, this proposed circuit is dedicated to propagates analog signals throughout the whole WaferIC. Our ADC samples the analog input signal using this proposed DAC with a successive approximation architecture. This digital signal is then propagated into a digital interconnection network and converted back to an analog signal at any other NanoPAds on the WaferIC with the same proposed DAC which suffers from the same non-linearity. Joint with a calibration method of the DAC, the same voltage level would be propagated through the WaferIC with respect of the precision of the proposed DAC.

Fig. 18 depicts a sine wave that was generated by the proposed DAC, for which the operating frequency is 23.5 Hz and the peak-to-peak amplitude is 1.479 V. A look-up table based code converter was used to address the DAC, configured to compensate the DAC non-linearity shown in Fig. 15. In order to apply a single DAC word configuration, the manufactured test chip requires 376 serially entered configuration bits. The serial mechanism that allows entering these bits in the test chip was successfully tested at a maximum frequency of 2.2 MHz. Due to test bench limitations of the test set-up, higher frequencies could not be test successfully. Moreover, the implemented DAC was designed to drive low integrated capacitive loads that are close to 1 pF. As a consequence, the settling time was approximated using two scope probes having different input capacitances (8 F and 12 pF). Indeed, by calculating the output capacitance of the DAC combined with the parasitics from the bonding of the package pins with the PCB trace, it was possible to estimate a more realistic output capacitance (see Table II).

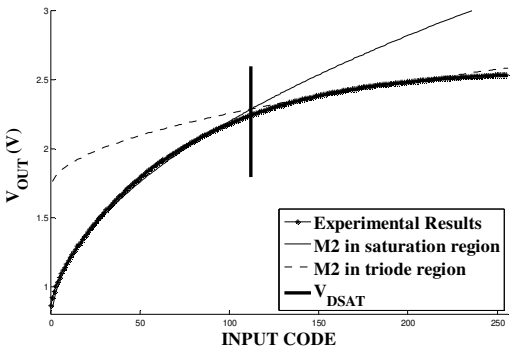

Fig. 15 Measured V_{OUT} for all digital inputs to the DAC.

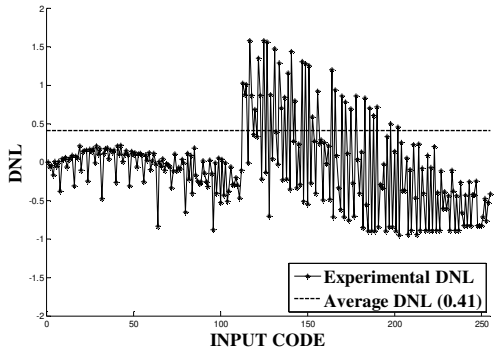

Fig. 16 Measured DNL of the proposed DAC where the average DNL is 0.41

Several measurements were performed and are shown in Table II, where an 8 pF and a 12 pF probe were used. From this table we can calculate that the capacitance associated with the parasitics and the DAC output has a value of 4 pF. According to the authors in [23], the package and the PCB parasitics can have a value of up to 8 pF. In [24] it is stated that a typical I/O pad, including the bonds, is typically around 5 pF. By calculation, we can assume that the parasitics from a PCB line have a value of around 3 pF. The settling time was thus computed by scaling the measured response time, using a 12 pF probe, to a 1 pF load (calculated as 4 pF minus 3 pF for the PCB line). This is a conservative approximation, since the calculated results still include the parasitics associated with the package bonding. The computed settling time ranges from 62.5 ns for 1 LSB to 100 ns for the full-scale operation, which corresponds, roughly, to a 10 MS/s DAC. This approximation is close to the post-layout simulation results, which excluded the package parasitics, and where a settling time closer to 20 ns was obtained.

Fig. 19 is the Fast Fourier Transform (FFT) extracted from the signal in Fig. 18. The corresponding Spurious Free Dynamic Range (SFDR) has a value of 42.31 dB. Using these results, a Signal to Noise Ratio (SNR) of 51.97 dB, a Total Harmonic Distortion (THD) of 49.52 dB, and a Signal-to-Noise and Distortion Ratio (SINAD) or 47.5dB can be computed. The corresponding Effective Number Of Bits (ENOB) is thus calculated to be equal to 7.6 bits.

The SNR, the TDH, and the SINAD were calculated as per [22] using (14), (15) and (16), and data from Table II.

The DAC calibration was performed using V_{ADJ} (Fig. 7) to increase or decrease the biasing voltage, such as to slightly decrease or increase the output voltage of the DAC. In a circuit reuse idea, as mention in the previous section, this voltage is to be set by another DAC of the 300k present on the WaferIC, acting as a reference voltage to set V_{ADJ}. The resulting output voltage variation of 25 mV is equivalent to about 4 LSB steps. Fig. 17 shows that when operating between 1.5 and 2.2 V, V_{ADJ} can be used to obtain a ±12.5 mV linear displacement of the DAC output. Fig. 17 also shows that the output voltage variations with respect to V_{ADJ} shows a good DC power supply rejection, thus ensuring that the output range will vary by the same offset when adjusting V_{ADJ}.

V. Comparison with Existing Work

Table III compares the work reported in this paper with recently published DAC architectures. In the context of wafer-scale integration, that is, to be able to integrate a network of over 150k DACs and 150k ADCs that can operate in parallel, the per-bit-size of the chosen design is a very important metric. The possibility of dynamically calibrating both DACs and ADCs is also vital, since process, voltage and temperature variations are large throughout a 200 mm wafer. The proposed architecture achieves a very small silicon area of less than 0.00035 mm^2/bit, which is almost 20 % smaller than the solution proposed in [25]. Furthermore, this is achieved without sacrificing the overall performance since the average DNL obtained is comparable to competing designs with an ENOB of 7.6.

Table II. Experimental results

Bit	Settling Time 12 pF (µs)	Settling Time 8 pF (µs)	Estimated Settling Time (ns)
MAX	1.6	1.2	100
Calculated V_{OUT} capacitance of 4 pF (16 pF total with probe)			
	Settling time 12 pF + 3pF+ 1pF (µs)		Estimated Settling Time 1pF(ns)
0 (LSB)	1.0		62.5
1	1.0		62.5
2	1.2		75.0
3	1.4		87.5
4	1.4		87.6
5	1.4		87.5
6	1.4		87.5
7 (MSB)	1.4		87.5
NOISE FLOOR: 58 dB		***fs*:10MS/s**	
Harmonic	Amplitude (dB)		
V1	-49.6		
V2	-50.8		
V3	-50.8		
V4	-52.4		
V5	-51.2		
SNR: 51.97 dB THD: 49.52 dB		**SINAD: 47.50 dB ENOB: 7.6 bits**	

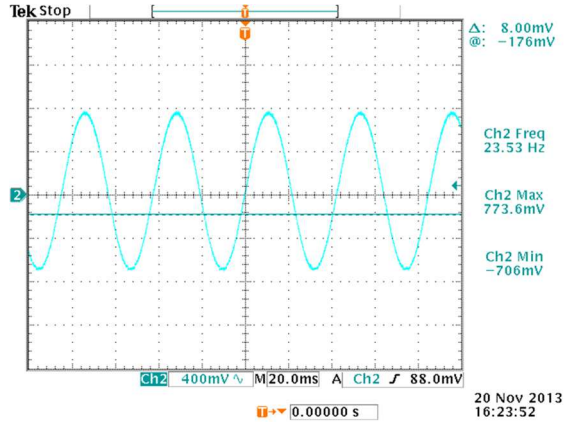

Fig. 18 Generated sine wave based on 256 points using the proposed DAC

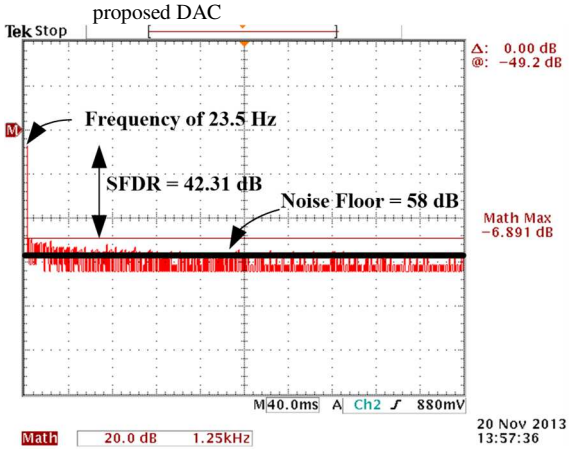

Fig. 19 Associated FFT of the sine waveform generated in Fig. 18 with 10k points.

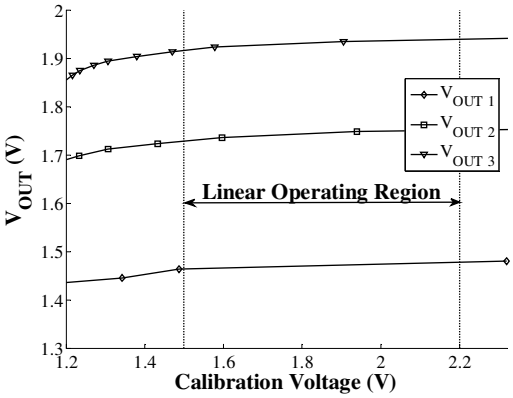

Fig. 17 Calibration range using V_{ADJ} signal in order to precisely set the DAC voltage output.

$$\text{SNR} = \text{NOISE FLOOR} - 10log_{10}\left(\frac{fs/2}{\text{BW}}\right) \quad (14)$$

$$\text{THD} = 20\log_{10}\sqrt{\left(10^{-V2/20}\right)^2 + \left(10^{-V3/20}\right)^2 + \ldots + \left(10^{-V5/20}\right)} \quad (15)$$

$$\text{SINAD} = 20\log_{10}\sqrt{\left(10^{-\text{SNR}/20}\right)^2 + \left(10^{-\text{THD}/20}\right)^2} \quad (16)$$

VI. Conclusion

In this paper, a novel approach was proposed for designing ADCs and DACs that are intended for wafer-scale integration. The resulting system, which employs a novel and very compact DAC architecture, allows for over 150k DACs and 150k ADCs to be interconnected with a fault tolerant network. Indeed, the converter grids can share their analog output to mitigate the impact of any fault encountered in the network.

The proposed DAC is based on an unbalancing technique that uses either a single or a multi-voltage reference to provide a wide selection of output voltages. Experimental results show that these DAC cover output voltages ranging between 864 mV and 2.538 V, with a resolution of 8 bits and a conversion speed of 10 MS/s. Moreover, an ENOB of 7.6 bits is achieved with an SNR of 51.97 dB and a SFDR of 42.31 dB. Finally, a dedicated dynamic calibration process allows for the DACs and ADCs to be fine-tuned to a range of 25 mV, thus allowing for any converter on the proposed network to be properly matched.

Table III. Comparison with existing works

	This Work	[9]	[26]	[27]
Technology	0.18 µm	0.13 µm	0.090 µm	0.18 µm
Year	2013	2016	2011	2012
Supply Voltage (V)	3.3	3.3	1.2/2.5	1.8
Resolution	8 bits	8 bits	12 bits	10 bits
DNL Average	0.41	N/A	<0.5	N/A
Speed	10MS/s	2MS/s	1.25GS/s	500 MS/s
Normalized Chip Size (mm^2)	0.00278	0.00099	3.3	0.034
Size Per Bit (mm_2)	0.00035	0.000012375	0.275	0.0034
ENOB	7.6	N/A	N/A	N/A
Calibration Process	YES	NO	YES	NO

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